Low Noise RF CMOS Receiver Integrated Circuits

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Low Noise RF CMOS Receiver

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SUMMARY

For a low-cost and fully-integrated chipset, a direct- conversion architecture has been widely used in wireless receivers. In addition, a standard complementary metal oxide semiconductor (CMOS) process has been broadly applied in implementations of wireless receivers because it is capable of high level integration with a baseband chipset. RF CMOS components for direct-conversion architectures offer not only a small-sized mobile terminal, but also a low-cost device with low power consumption. Moreover, for practical versatility, wideband RF CMOS components need to be used in high data-rate applications, such as 4G wireless communications, and multi-standard applications. For these applications, the noise of the RF components needs to be designed as low as possible since the mobile terminals for these applications require high signal-to-noise ratio (SNR) performance.

The objective of this research is to design and implement low-noise wideband RFIC components with CMOS technology for the direct-conversion architecture. This research proposes noise reduction techniques to improve the thermal noise and flicker noise contribution of a low noise amplifier (LNA) and a mixer. Of these techniques, the LNA is found to reduce noise, boost gain, and consume a relatively low amount of power without sacrificing the wideband and linearity advantages of a conventional common gate (CG) topology. The research concludes by investigating the proposed mixer topology, which senses and compensates local oscillator (LO) phase mismatches, the dominant cause of flicker noise.

I. INTRODUCTION

1.1. Background

Recently, many kinds of wireless communication systems have been produced and studied for their different applications. Various demands from consumers have promoted the development of multiple wireless standards. For example, global system for mobile (GSM), code division multiple access (CDMA), and wideband CDMA (WCDMA) are used for voice and relatively low data rate communications, while local wireless area networks (WLANs) and worldwide interoperability for microwave access (WiMAX) focus mainly on high data rate communications in nomadic environments, as shown in Figure 1.1. For future wireless communication systems, such as cognitive radio (CR) systems and 4^{th} generation (4G) communication systems, a variety of services will need to be supported. From existing wireless systems, users are able to manage their email and surf the Web, but their demands may not be limited to only these. They may want to download multimedia services and communicate real-time video telephony on their wireless mobile terminal even in a high speed mobility environment. Thus, with the move to the next generation of wireless mobile systems, new communication standards have to provide higher data rates to accommodate the needs of the users.

Various modem techniques have been suggested to achieve a high data rate in wireless communication systems. Because the information date rate is restricted by the channel bandwidth of the radio signal, the simplest way to enhance the data rate is by increasing the channel bandwidth. However, the increased bandwidth consumes a large amount of

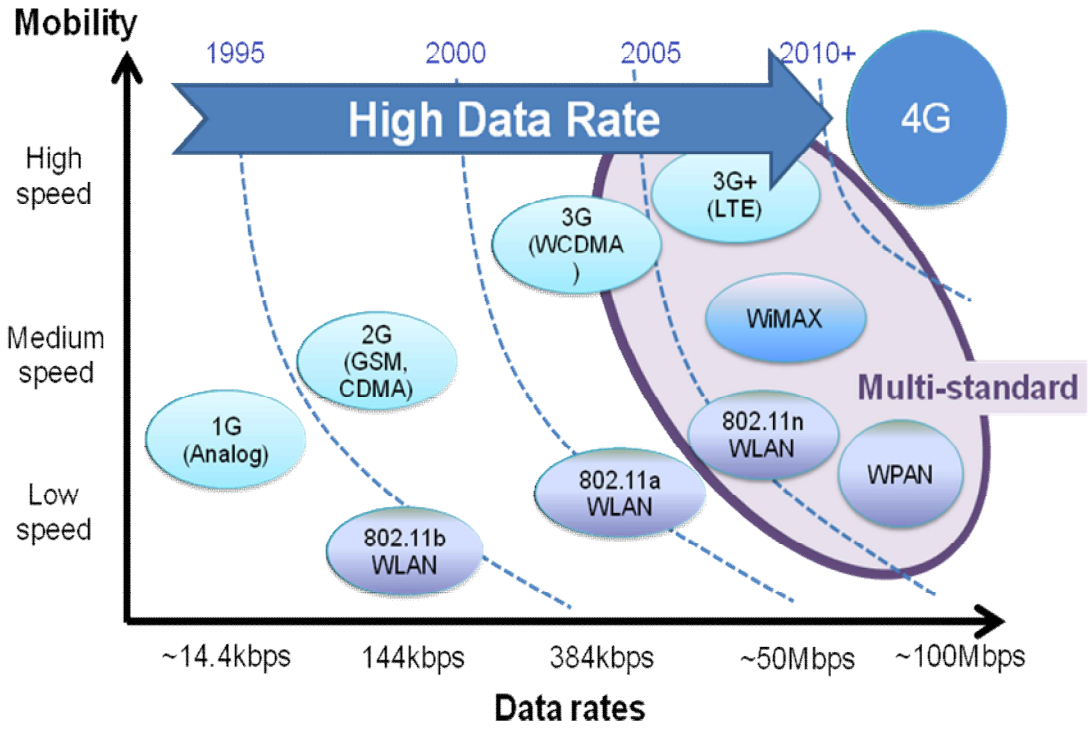


Figure 1.1 : The evolution of modern wireless communication systems

frequency resources, which then restricts the number of users. In addition, a wide bandwidth transmission signal is often disturbed by selective fading, which makes the signal difficult to recover. Moreover, in high speed mobility, as the channel condition is fluctuated greatly, the wide channel bandwidth makes it difficult to estimate the response of the channel.

When the fixed channel bandwidth is considered, one of candidates to increase data rate is a large constellation size, shown in Figure 1.2. In modern wireless communication systems, a quadrature amplitude modulation (QAM) is widely used as a modulation scheme since it provides larger spaces between constellation symbols than phase-shift keying (PSK) and amplitude-shift keying (ASK) in a given energy. The large data

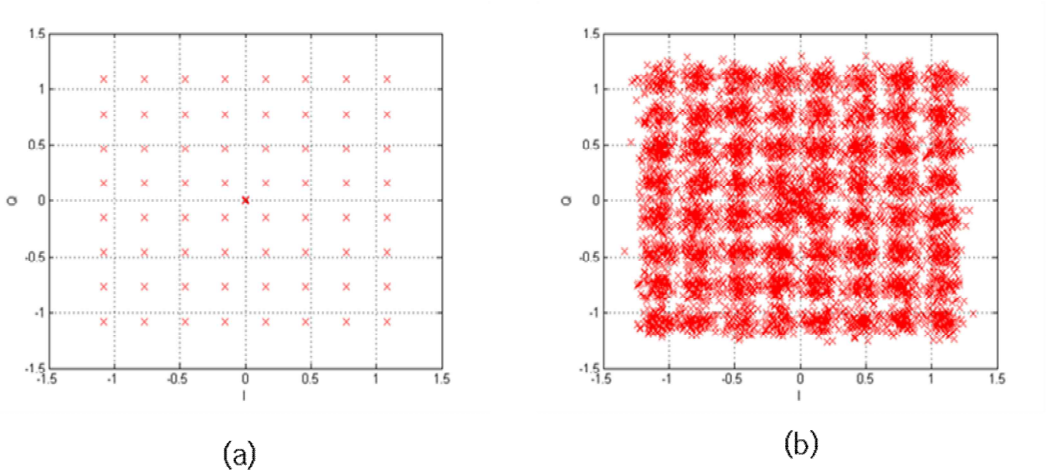


Figure 1.2 : The 64QAM modulation (a) ideal constellation (b) constellation with low SNR.

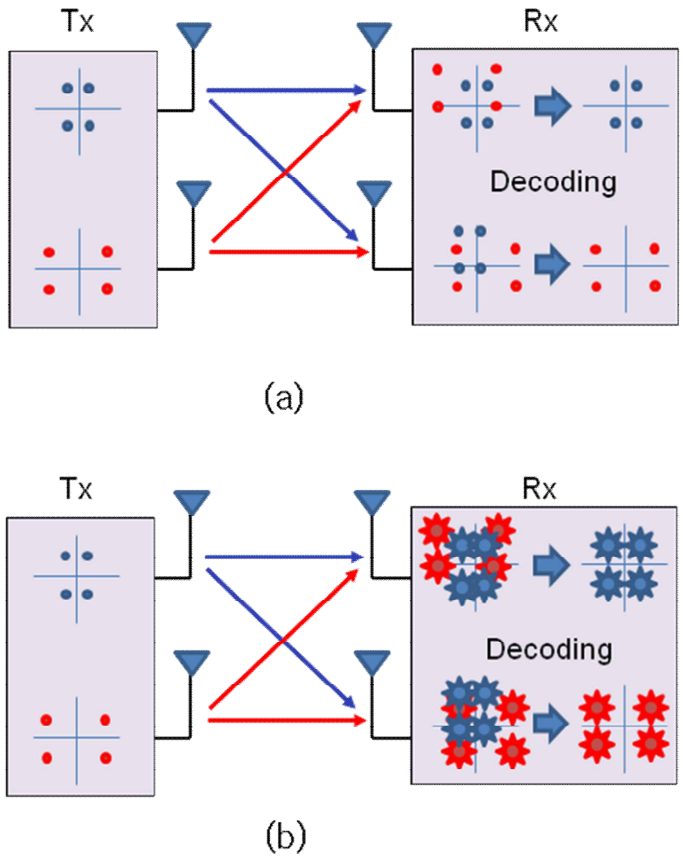


Figure 1.3 : 2-by-2 MIMO spatial multiplexing (a) with high SNR (b) with low SNR.

mapping size of QAM, for example, 64 QAM instead of 16QAM, can increase the data rate in the given bandwidth because it offers a high bits per symbol rate. In addition, a MIMO (Multiple-Input Multiple-Output) spatial multiplexing technique can maximize the average channel capacity, shown in Figure 1.3. The MIMO technique also increases the data rate by transmitting and receiving independent information on different antennas in the same channel bandwidth. However, a low signal to noise ratio (SNR) of receivers decreases the data rate in both cases. When the SNR of the receivers is not sufficient, constellation errors of de-mapping are generated due to noise. The large constellation mapping/de-mapping size is vulnerable to these errors because the constellation distance is relatively short. In addition, the bit error rate (BER) performance of the MIMO technique is also degraded with a low SNR condition. This is because the constellation error in one antenna path can degrade the decoding performance of other paths as well as that of its own path. Therefore, high SNR performance is prerequisite for high data rate communication in mobile terminal receivers.

1.2. Motivation

For systematic analysis of the SNR in the receiver, a sensitivity equation, given below, served as a useful starting point.

$$Sensitivity = -174\,dBm/Hz + 10\log(BW) + NF + SNR_{System}, \qquad (1.1)$$

where BW is the channel bandwidth in Hz, and NF is the noise figure of the RF parts. The sensitivity implies minimum received power for having SNR_{System}, and the first two terms of the right-hand side in (1.1) indicates the noise floor of the system. To have high SNR for the system, either increased received power or a decreased noise floor is necessary. In

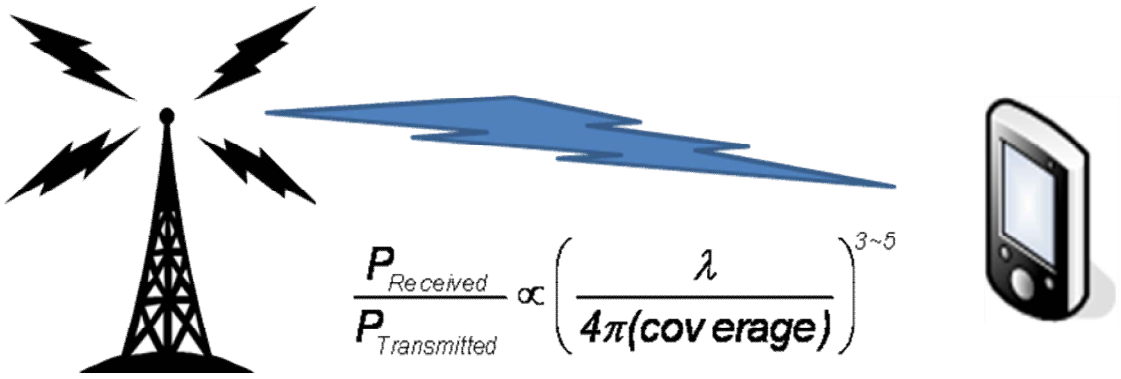


Figure 1.4 : The characteristics of path loss.

the first case, to increase received power, the coverage needs to be reduced or transmitted power should be increased from the path loss equation shown in Figure 1.4. Reduced coverage implies high cost which will result from the increased number of required base stations. Not only would be the cost be higher, but, any increased transmitted power is currently restricted by out-of-band power spectrum regulation from communication standards. On the other hand, to decrease the noise floor, the channel bandwidth can be decreased, which then decreases the data rate. These two methods for enhancing the SNR of the systems come with many drawbacks. However, one efficient way to increase the SNR of the system is to minimize the noise figure in the RF parts in the given received power with the given bandwidth.

Another cause of increased future demand on wireless communication systems, many users may hope to use just one terminal device, supporting multiple wireless standards, for their convenience. The demand of users emphasizes the need for the convergence of various applications on a single chipset for wireless communication mobile terminals. However, from a radio frequency (RF) portion standpoint, the integration of various applications must include careful consideration of system budgets, including both cost and area. For example, parallel placements of an independent RF transceiver path for

each application increase the total chip area and power consumption. To minimize these problems, RF components need to operate in a wide bandwidth covering different applications at the same time.

1.3. Organization of the Thesis

Based on the technological background and motivation, the purpose of this work is to implement low noise wideband RF receivers for high-data-rate and multi-standards wireless mobile communications. This dissertation consists of six chapters.

To provide background for the research, Chapter 2 presents an explanation of the basic concepts of RF receiver architectures for wireless communications. With the implementation of direct-conversion RF receivers in a CMOS technology, the noise sources including thermal and flicker noise are discussed. Also presented are key RF building blocks for noise contribution of RF receivers.

Chapter 3 proposes a low noise and high gain wideband LNA for reducing thermal noise contribution in RF receivers. The operation and performance of the proposed LNA is introduced with an analysis of gain, stability, noise figure, and linearity.

Chapter 4 discusses the effect of flicker noise on communication systems. It proposes a new flicker noise model for the system simulation with an OFDM PHY layer and measures the model's effect on the system. The performance of the model with a channel-coding scheme is also tested in order to evaluate its noise reducing effect on the system.

Chapter 5 represents a low-flicker noise mixer topology for reducing flicker noise contributions in RF receivers. The mechanisms of flicker noise generation in the mixer are introduced, and a new concept for flicker noise reduction is explained. The enhanced flicker noise performance of the mixer is compared with that of conventional Gilbert-cell mixers.

Finally, Chapter 6 summarizes the research findings, and makes conclusions about this dissertation.

II. LOW-NOISE CMOS RF RECEIVERS

2.1. Introduction

In order to advance into the topic of low-noise CMOS RF receivers, general RF receiver architectures need to be discussed in advance for the rest of these researches. Understanding the operation of the each RF architecture and the pros and cons of it is prerequisite for designing a RF receiver. Among various RF architectures, the direct-conversion architecture is noteworthy for future wireless communication mobile terminals because it offers low-cost implementation. However, this architecture can provide a high noise issue, which is not crucial in other architectures. In the implementation of a CMOS technology for cost saving, the noise contribution of the direct-conversion architecture is even more important to realize high performance RF receivers.

In Section 2.2, the characteristics of RF receiver architectures, such as heterodyne type and direct-conversion type, are introduced. The noise sources in CMOS technology including thermal noise and flicker noise are discussed in Section 2.3. Finally, key RF building blocks for low-noise contribution in the CMOS direct-conversion RF architecture are discussed in Section 2.4.

2.2. RF receiver Architectures

2.2.1 Heterodyne architectures

The RF receiver architectures are generally classified as heterodyne types and direct-conversion types. In the heterodyne architectures, the incoming RF signal is down-

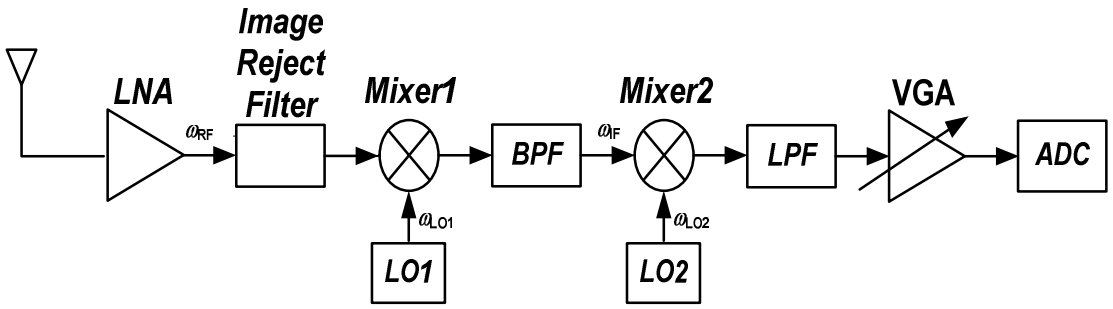


Figure 2.1: The Heterodyne architecture.

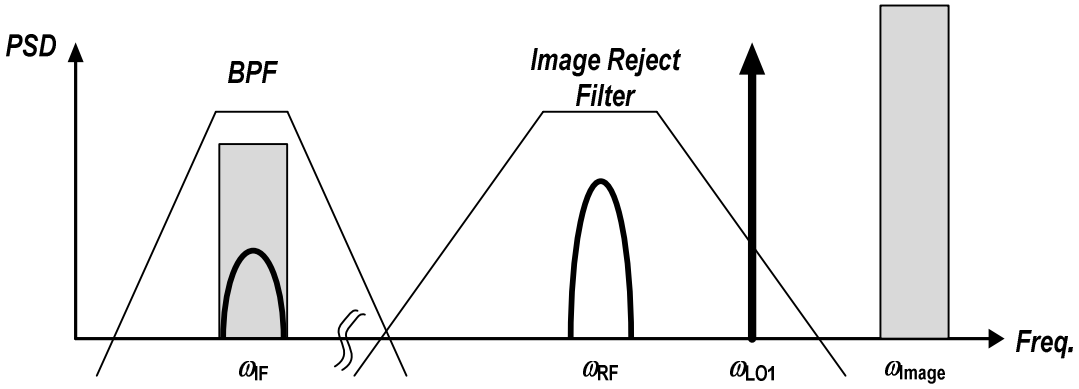


Figure 2.2: The Image problems in the heterodyne architecture.

converted to intermediate frequency (IF), and then the IF frequency is converted to DC frequency. The frequency conversion process is carried out by a mixer and a local oscillator (LO), shown in Figure 2.1. The RF frequency, ω_{RF}, is first mixed with the first LO frequency, ω_{LO1}, and the mixing process produces two frequency signals in $\omega_{RF} + \omega_{LO1}$ and $\omega_{RF} - \omega_{LO1}$ when the harmonic signals according to non-linear function of the mixer are ignored. The following band-pass filter (BPF) then choose IF frequency, $\omega_{IF} = \omega_{RF} - \omega_{LO1}$, when low side band LO injection is supposed. The second mixing process by means of the second mixer and LO translate the IF signal to near DC frequency signal for analog-to-digital conversion processing. The IF conversion plays a vital role in the performance of the overall RF systems. The IF component enhances the selectivity of the

system since it provides a high out-of-band rejection ratio. In addition, the heterodyne receiver has high stability because the dual mixing process produces high isolation between previous and following RF building blocks.

In spite of these advantages, the heterodyne receiver suffers from performance degradation according to image bands. The image bands, which is located in $\omega_{LO1} + \omega_{RF}$, are also down-converted to the IF frequency, shown in Figure 2.2. This image bands are regards as noise or interferes from the viewpoint of IF signal. The power of image bands can be much higher than that of desired signal because each wireless terminal may have no control over the signals in other bands. Therefore, image rejection filter, which is inserted between LNA and mixer for suppressing the image, is mandatory in heterodyne receiver.

2.2.2 Direct-conversion architectures

On the other hand, the direct-conversion architecture has been widely used in modern wireless RF receivers because it can eliminate the image rejection filter. The direct-conversion architecture is simply translated to the baseband by using only the first down-conversion, where the LO frequency is equal to the RF frequency, shown in Figure 2.3. Thus, the image problem is avoided because $\omega_{IF} = 0$. The image rejection filter in the heterodyne receiver is implemented by off-chip components such as surface acoustic wave (SAW) devices to have a high image rejection ratio. Thus, the direct-conversion receiver without the image rejection filter can be a potential solution of a low-cost and fully integrated chipset. In addition, the LNA doesn't need to drive 50Ω load since the filter is not required at the output of the LNA. Thus, the voltage gain of the RF front-end

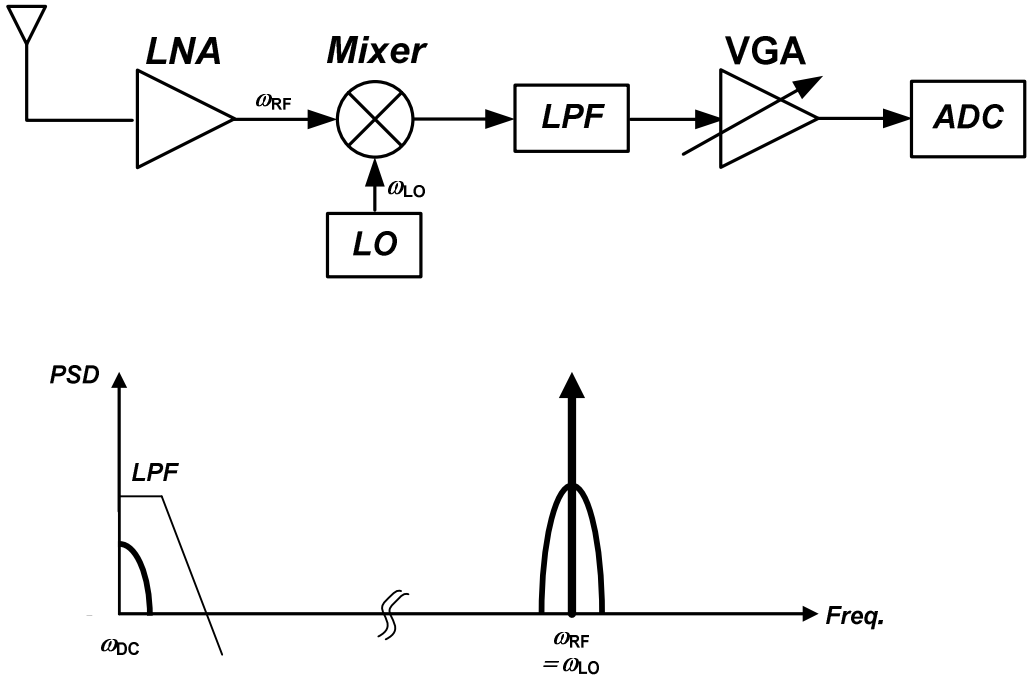


Figure 2.3: Direct conversion architecture.

can be enhanced. Moreover, the noise figure degradation in the heterodyne receiver due to the image bands can be solved. However, the direct-conversion architecture imposes many other issues, which are not serious in heterodyne architectures. First, a DC offset voltage is one of important problems in the direct-conversion receiver because the offset voltage can corrupt the signal and saturate the following stages. The DC offset is originated from LO leakages, second order harmonics, and device mismatches in RF receivers. The LO leakages are generated when the isolation between the LO port and the RF port of the mixer is not sufficient. The deficient isolation between these two ports is arisen from capacitive substrate coupling. Due to the LO leakage, a finite amount of feedthrough signal exists from LO port to the input of previous stages, shown in Figure 2.4. The LO leakages at the input of the previous stages are mixed with the LO signal, is

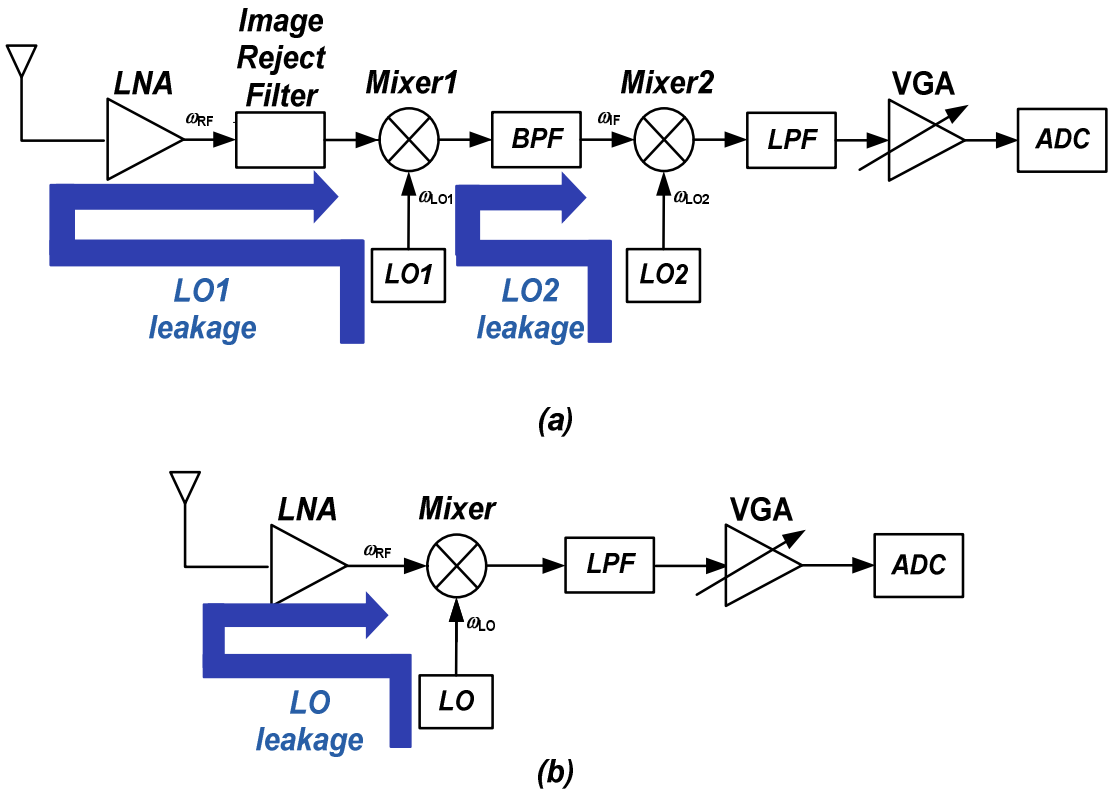


Figure 2.4: (a) LO feedthrough in heterodyne receiver (b) LO feedthrough in direct conversion receiver architecture.

thus producing a DC offset component. This phenomenon, normally named as self-mixing, is occurred both in the heterodyne and in the direct-conversion architecture. However, in the heterodyne receiver, the LO leakage from the first local oscillator (LO1) sufficiently degraded by the image rejection filter, and then the DC offset according to LO1 leakage is not appeared at IF stages. In addition, the second local oscillator (LO2) leakage is suppressed by band pass filter (BPF). In addition, The LO2 leakage is much lower than the LO1 leakage. It is because that the frequency of LO2 is much lower than that of LO1, and then the low-frequency components suffer from low parasitic and substrate coupling. From these reasons, the LO leakages do not much contribute to DC

offset in the heterodyne receiver, whereas the LO leakage is crucial in the direct-conversion receiver.

The second order harmonics produce DC offset voltages as well. The signal of non-linear components, such as LNA and mixer, are characterized by power series coefficients g_1, g_2, g_3. In this case, the output signal, $y(t)$, is calculated from input signals, $x(t)$, as follows.

$$y(t) = g_1 x(t) + g_2 x(t)^2 + g_3 x(t)^3 + \ldots. \tag{2.1}$$

If $x(t) = A\cos(\omega_{RF} t)$, then second order term in (2.1) is

$$\text{sec}\,ondy\ order\ y(t) = g_2[A\cos(\omega_{RF} t)]^2 = g_2 A^2[\frac{1+\cos(2\omega_{RF} t)}{2}]. \tag{2.2}$$

Thus, the output signal includes DC term, indicating that second order harmonic of non-linear component generates DC offset. In addition, the device mismatches in differential configurations lead to DC offset. If the differential input voltage is zero and the differential devices are perfectly symmetry, $V_{OUT} = 0$, but in the presence of mismatches,

$$V_{OUT} = A_V \times V_{OS}, \tag{2.3}$$

where A_V is voltage gain of the circuits and V_{OS} is the DC offset voltage.

The DC offset voltages from second order harmonics and device mismatches are much severe problem in the direct-conversion receiver. Referring again to Figure 2.4, the required total gain from the antenna to the input of ADC is generally around 80dB to 100dB in order to amplify small input signal, which has the power level of sensitivity, to full scaled power for ADC. Of the gain, the LNA/Mixer parts typically contribute to 20 to 30dB. It is because that these components contribute high noise to the cascade system at low levels of gain, whereas they add distortion at high levels of gain. Therefore, the

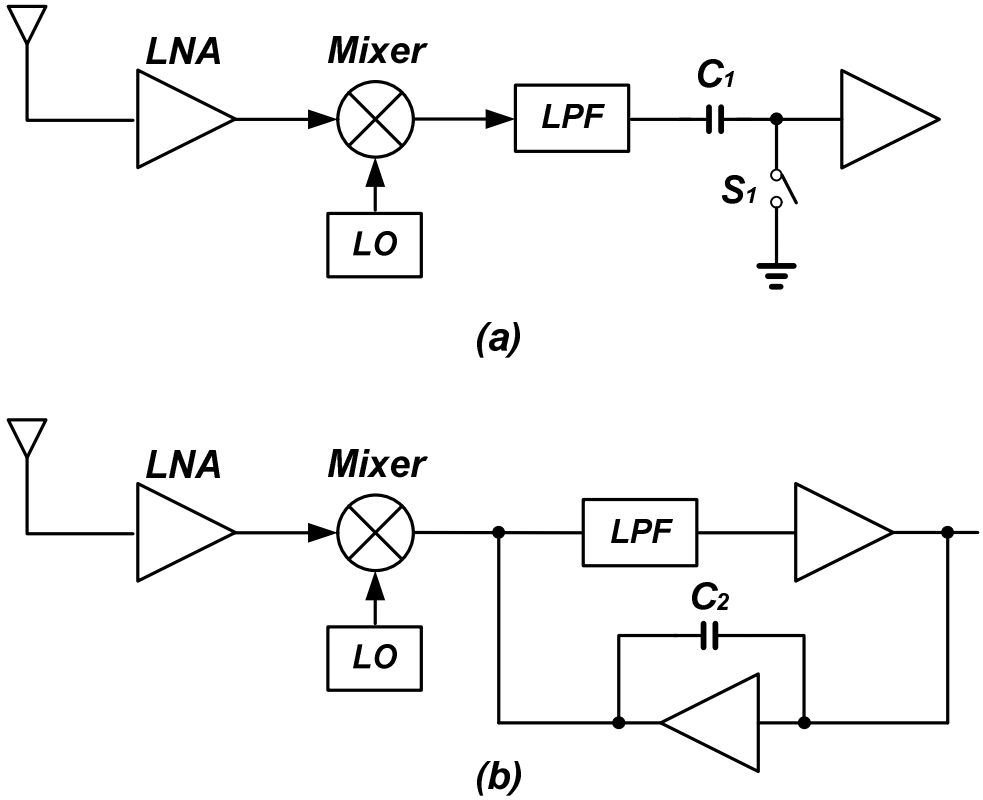


Figure 2.5: (a) DC offset cancellation in TDD mode (b) DC offset cancellation with a large capacitance

required gain after DC frequency conversion in direct-conversion receiver is much higher than in heterodyne receiver, which has an additional mixing stage to enhance the gain. Therefore, when the same amount of DC offset voltage generation is supposed in both architectures, the direct-conversion receiver produces much larger DC offset voltage due to its high DC gain.

Even though the DC offset problem is critical to implement the direct-conversion receiver, several offset cancellation techniques, consuming cost and area, have been reported. Shown in Figure 2.5. (a). is one of examples. The switch, S_1, turns on during idle time to store the offset voltage in a capacitor, C_1. During the reception of data, S_1

turns off, and then the configuration performs offset cancellation. However, this offset cancellation technique is only useful in time division duplex (TDD) mode applications because it needs idle for a certain time. On the other hand, high pass filtering can be solution for DC offset cancellation, shown in Figure 2.5 (b). The combination of an OP amplifier and a capacitor, C_2, senses DC offset voltage, and then cancels out the offset. Even though this offset cancellation technique can utilize in both TDD and FDD mode, it requires a very large capacitance of C_2. The large capacitance brings large settling time to cancel offset voltage, and occupies a large silicon area.

As a result, the DC offset problem in the direct-conversion receiver can be alleviated by several circuit techniques. However, a flicker noise issue is severe to compensate by using circuit techniques. As mentioned earlier, the required gain after DC frequency conversion is relatively high in the direct-conversion receiver. The high DC gain implies that many cascade gain stages are required. A large number of gain stages accompany a large flicker noise since each gain stage contributes to flicker noise. Thus, flicker noise is key issue in the direct-conversion architecture.

2.3. Noise sources in CMOS RF receiver

Nowadays, CMOS technology is widely used for most of RF building blocks implementation. Especially, in RF receivers for modern wireless communication systems, all of the active RF building blocks are implemented by CMOS technology. It is because that the CMOS technology is capable of integration with a baseband chipset and offers low-cost implementation. Therefore, the CMOS technology and the direct-conversion architecture are welcomed for its great versatility and cost-effective view point. However,

the commercialization of low-noise CMOS RF receiver with the direct conversion architecture has not been easily achieved by the intrinsic drawbacks of standard CMOS processes in RF perspectives, that is, a low transconductance, low unit gain frequency (f_T), and high flicker noise. The low values of transconductance and f_T provide high thermal noise. In this section, thermal noise and flicker noise in CMOS technology is discussed.

2.3.1 Thermal noise

It is widely accepted that thermal noise of the MOS transistor is generated from gate noise, gate induced noise, and channel noise, shown in Figure 2.6 (a). If these noise sources are correlated, overall noise of MOS transistor is reduced. The gate noise arises from ohmic resistance of the gate material. As the gate, source, and drain materials exhibit finite resistivity, the resistance of each port can contribute to noise. When we suppose that the MOS transistor is relatively wide, the source and drain resistance can be negligible due to its large contact area. However, the gate resistance is relatively high because of restricted small gate area. This gate resistance can be reduced by a parallel structure. With the help of this structure, named as multi-finger configuration, the overall resistance is distributed in each small resistance, shown in Figure 2.6 (b). The noise generated from the each gate resistance is connected in parallel and then overall gate noise can be reduced. Therefore, this research does not consider gate noise because the effect of the noise is reduced by proper layout.

The one of the other thermal noise sources in MOS transistor is gate induced noise. The phase delay of the channel formation couples into the gate terminal with miller

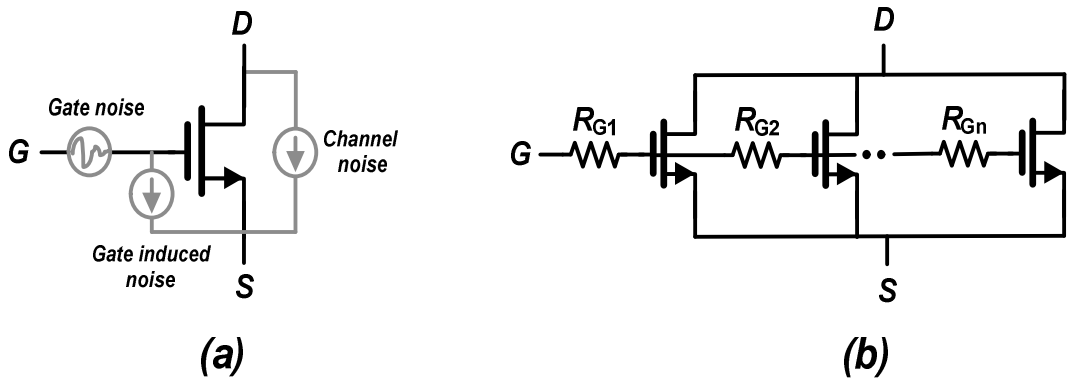


Figure 2.6: (a) Thermal noise sources in MOS transistors (b) gate resistance distribution

capacitance, resulting in a gate-to-source noise current. This gate induced noise is expressed as

$$\overline{I_n^2} = 4kT\delta g_g \,, \tag{2.4}$$

Where g_g is

$$g_g = \frac{\omega^2 C_{gs}^{\ 2}}{5g_{d0}} \,. \text{ [1]} \tag{2.5}$$

The parameter of g_{d0} is the drain-source conductance at zero drain-to-source DC voltage. The typical value of δ is 4/3 for long channel devices and this equivalent noise model shows in Figure 2.7 (a). From (2.4) and (2.5), the gate induced noise current increases with frequency. Thus, this noise source deeply impacts on high frequency operation. For a certain frequency, the noise current can be converted to the noise voltage source with a resistive component, as shown in Figure 2.7. (b) [2]. In this case, when the Q value of C_{gs}

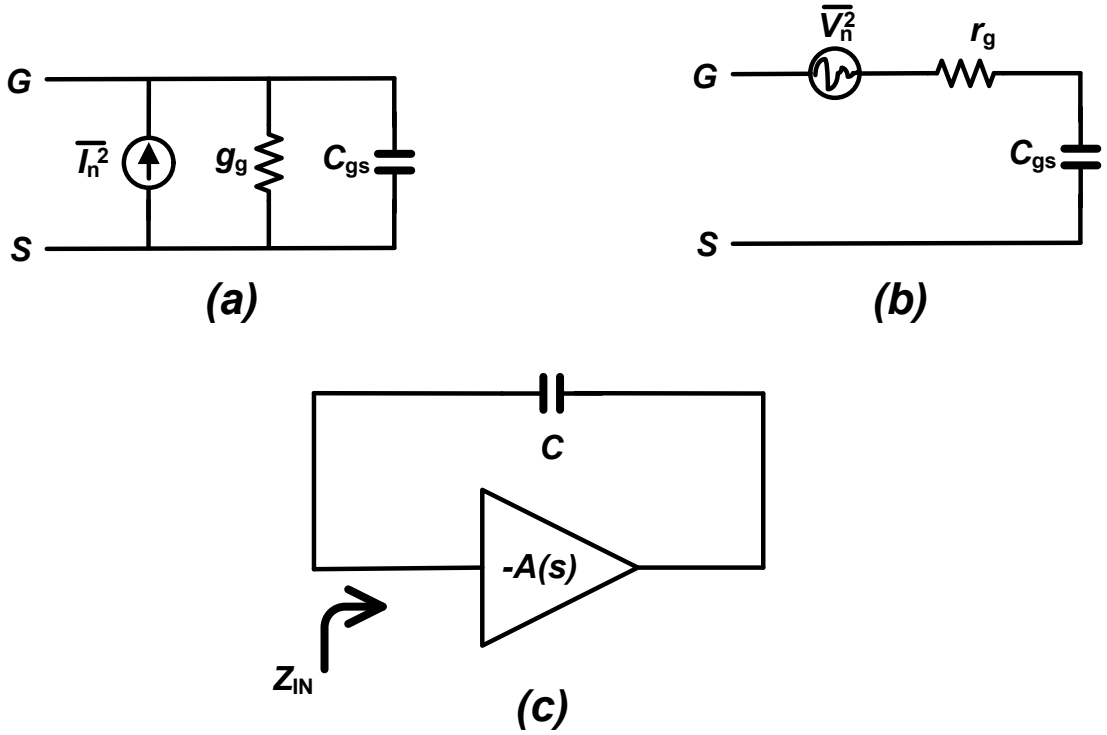


Figure 2.7: (a) Gate induced noise model (b) Alternative gate induced noise model (c) Miller capacitance model.

is sufficiently high, the gate resistance is given as

$$r_g = \frac{1}{5g_{d0}} = \frac{\alpha}{5g_m}. \tag{2.6}$$

The α. is defined as the ratio of g_m and the zero bias drain conductance g_{d0}. In long channel devices, the typical r_g value is around 5 to 10 Ω when high frequency operation is supposed. The r_g value contributes input matching as well as noise sources. The mechanism of the gate induce noise source is generally explained by miller capacitor model, shown in Figure 2.7 (c). This model consists of the amplifier having a frequency dependant gain, *A(s),* and the feedback capacitance between input and output. The input port of the model supposes the gate terminal and the output port of it implies the channel. In this case, the input impedance of this circuit is

$$Z_{IN} = \frac{1}{sC(1+A(s))}. \tag{2.7}$$

For the high frequency operation, carrier velocity in the channel of the MOS transistor can be slower than applied gate input signal velocity in the MOS transistor. In that case, the phase difference between the input and output port exhibits. Thus, input impedance equation in (2.7) needs to be modified as

$$Z_{IN} = \frac{1}{sC(1+A_0 e^{-j\phi})} = \frac{1}{j\omega C(1+A_0\cos\phi)+A_0\omega C\sin\phi}. \tag{2.8}$$

From (2.8), the input impedance of the circuit model possesses real part admittance. The real admittance implies that the model possesses the shunt conductance, which can generate noise. This value of shunt conductance increases with frequency. Therefore, the phenomenon of this model is same as the explanation from (2.4) and (2.5). However, the gate induced noise acts as a dominant noise source in only high frequency operation. Thus, this research does not take into account the gate induced noise because the noise can be negligible in interested a low frequency or moderate frequency circuit operation.

The most important thermal noise source is channel noise. This noise is independent of frequency and can be modeled by a current source connected between the drain and source terminals with a spectral density.

$$\overline{I_n^2} = 4kT\gamma g_{d0} = \frac{4kT\gamma g_m}{\alpha}, \tag{2.9}$$

where γ is the thermal noise coefficient of the MOS transistors. The coefficient γ is equal to 2/3 for long-channel devices and the value becomes larger for submicron MOS devices. Replacing (2.9) to input-referred noise voltage, it is given as

$$\overline{V_n^2} = \frac{4kT\gamma g_m}{\alpha g_m^2} = \frac{4kT\gamma}{\alpha g_m}. \tag{2.10}$$

In the submicron MOS devices, even though the coefficient γ increases, the value of g_m even more increases. Therefore, as the gate length becomes smaller, the overall input-referred channel noise decrease. As the channel noise is the dominant noise source in CMOS devices for normal frequency operation and typical g_m value, this research only considers the channel noise as thermal noise sources.

As the channel noise is critical to thermal noise sources in MOS transistors, the amount of the noise can be compared with that of shot noise, which is the dominant noise source in BJT transistors. The shot noise in BJT devices is given as

$$\overline{I_n^2} = 2qI_{DC}, \tag{2.11}$$

where q is the electronic charge, and I_{DC} is the DC current in amperes. The shot noise is also white, implying frequency independency. The (2.11) can be replaced to input-referred noise voltage, and it is given as

$$\overline{V_n^2} = \frac{2qI_{DC}}{g_m^2}. \tag{2.12}$$

In BJT devices, $g_m = I_{DC} / V_{th}$, and then

$$\overline{V_n^2} = \frac{2qV_{th}^2}{I_{DC}}. \tag{2.13}$$

The input-referred shot noise in BJT transistor from (2.13) is inversely proportional to $I_{DC,}$ while input-referred channel noise in MOS from (2.10) is inversely proportional

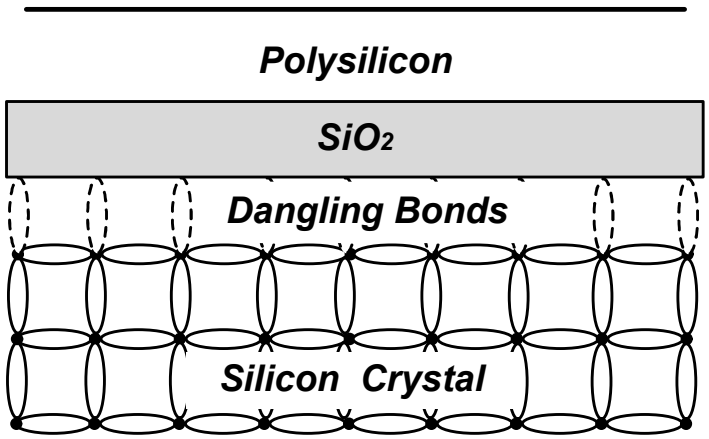


Figure 2.8: Dangling bonds in a Si-SiO2 interface.

to $g_{m.}$ The value of g_m is proportional to $sqrt(I_{DC})$ in CMOS transistors. Therefore, the thermal noise of CMOS transistors is much higher than that of BJT transistors.

2.3.2 Flicker nose

Flicker noise, typically referred as 1/f noise, dominates low-frequency noise. The noise spectral density of the noise is inversely proportional to frequency. Flicker noise not only occurs in electrical systems. It can be observed in biological systems, in fluctuations of the frequency of rotation of the earth, and in the fluctuations of variables in economics [3]. Therefore, flicker noise is a systematic effect inherent in all physical processes. In wireless communication system, flicker noise degrades signal to noise ratio (SNR) of the system in low frequency. However, there are no universal mechanisms to exactly describe flicker noise phenomenon. In CMOS technology, a charge trapping and releasing model is generally accepted [4]. This model is illustrated in Figure 2.8. At the end of interface of silicon crystal in CMOS transistor, many dangling bonds appear according to the defects and impurity in the surface. The dangling bonds generate extra energy state and they randomly trap and release the charge carrier [5]. This phenomenon

generally occurs at low frequency more often, and then 1/f noise spectrum characteristics are generated. From this model, the reason that flicker noise of MOS devices is higher than that of BJT devices is explained. MOS devices are surface oriented and BJT devices are buried oriented. As the defects and impurity occurs more often in the device surface, MOS devices present more flicker noise.

The other mechanisms are also introduced to generate flicker noise. The carrier density fluctuation model, introduced by McWorther [6], explains that flicker noise is generated from the fluctuation of channel free carriers in the Si-SiO_2 interface. The model expresses that flicker noise is independent of the gate bias voltage, and the magnitude of the noise is proportional to the interface density. In addition, the mobility fluctuation model, suggested by Hooge [7], illustrates the dependence of flicker noise on high gate bias.

Flicker noise of the MOS device is modeled by a noise voltage source in the gate terminal with a series connection and given by

$$\overline{V_n^2} = \frac{KI_{DC}}{C_{OX}WL}\frac{1}{f^n}, \tag{2.14}$$

where K is the flicker noise coefficient, and I_{DC} is the dc current. The value of n is normally approximated as a unity for easy calculation. From (2.14), the large device area, WL, can reduce flicker noise. It is because that the large gate capacitance, which is driven from the large device size, smoothes the channel fluctuation of the MOS transistor. In addition, the DC current is proportional to flicker noise. Thus, the MOS transistor design of a large device size with a small bias current can improve the flicker noise effect. The K value of PMOS transistor is much lower, around 50 times, than that of NMOS transistor

[4]. Therefore, the use of PMOS transistor instead of NMOS is beneficial to flicker noise reduction, whereas it has degraded transconductance due to its low mobility.

2.4. Key RF building blocks for low-noise CMOS RF receiver

As discussed earlier, the direct-conversion RF receiver is easily vulnerable to flicker noise. In addition, the RF receiver with CMOS technology provides higher thermal noise as well as higher flicker noise than receivers with other technologies. In the direct-conversion CMOS RF receiver, the most critical building block for thermal and flicker noise can be determined as follow.

2.4.1 Thermal nose

For direct-conversion architectures, which compose of a cascade of RF building block, overall thermal noise can be obtained in terms of the noise figure and gain of each stage. Consider again the direct-conversion receiver architectures, shown in Figure 2.9. The overall noise figure according to thermal noise can be driven from Friss equation [8].

$$NF_{System} = NF_1 + \frac{NF_2 - 1}{G_{P1}} + ... + \frac{NF_M - 1}{G_{P1}...G_{P(M-1)}}, \tag{2.15}$$

where NF is the noise figure of the *m-th* stage and G_{P1} is the available power gain of the *m-th* stage. The available power gain is defined as the available power at the output divided by the available source power. In the special case where the input and output impedance of each stage are same, the available power gain can be replaced with voltage gain. The Friis equation expresses that the noise contribution of each stage decreases as the gain of the preceding stage increases. This fact implies that the first few stages in a cascade are the most critical to overall system noise figure. From

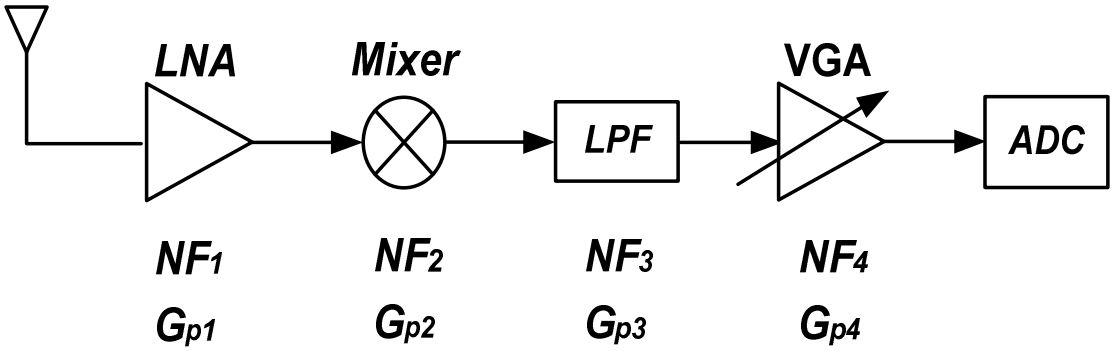


Figure 2.9: Direct conversion architecture with gain and noise figure.

these results, we can conclude that low noise figure and high gain of LNA is critical to thermal noise of overall system.

2.4.2 Flicker nose

As mentioned earlier, the RF building blocks after DC frequency conversion can contribute to flicker noise. Referring again from Figure 2.9, the down conversion mixer, filter, and VGA are flicker noise sources in the direct-conversion receiver. These RF building blocks can be classified as switching devices, such as the mixer, and non-switching devices, such as the filter and VGA. The research of [9] represents that switching devices have higher flicker noise than non-switching devices when switching frequency is higher than output bandwidth. In the direct-conversion receiver, the switching frequency of the mixer is the same as the RF input frequency, which approximates as a few GHz. In addition, the output bandwidth of the mixer is under 100MHz for applying most wireless communication systems. Thus, flicker noise of the mixer in the direct-conversion receiver is higher than that of other RF building blocks. As

a consequence, the LNA is critical building block for the contribution of thermal noise, and the down conversion mixer is dominant for the contribution of flicker noise.

III. LOW NOISE WIDEBAND CMOS LNA DESIGN

3.1. Introduction

From previous discussion, the performance improvement of noise figure and gain is essential in LNA design to achieve low thermal noise characteristics for high data rate communications. In addition, the LNA needs to operate in a wide bandwidth and high linear for multi-standard application. For accepting various applications at the same time, the wideband design of the LNA is efficient way in cost and area. However, the wideband LNA is vulnerable to interferers generated from unwanted other applications because the power of in-band interferers are not reduced by preceding filters. Thus, for applying multi-standards applications, the wideband and high linear is crucial characteristics of the LNA design. Moreover, power consumption of the LNA needs to be minimized for adapting a mobile terminal efficiently. Normally, in the LNA design from conventional topologies, most of these specifications have trade-off relation with each other, shown in Figure 3.1. Therefore, in this research, a LNA having high performance of these specifications simultaneously is proposed through a new concept of topology.

In Section 3.2, the conventional topologies for wideband LNA is explained. The gain boosting technique for common gate wideband LNA topology is also presented. Section 3.3 and Section 3.4 represent concept and implementation of the proposed LNA, respectively. The proposed wideband LNA provides the characteristics of high gain, low noise, and low power consumption. Section 3.5 illustrates the analysis of the LNA with the viewpoint of gain, stability, noise, and linearity. The experimental results of the LNA

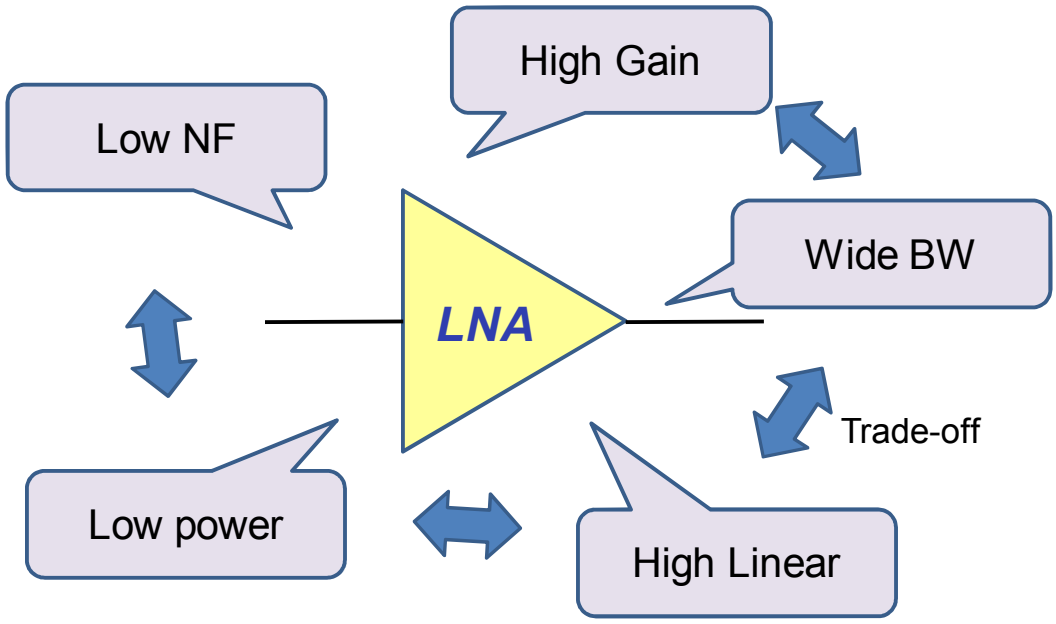


Figure 3.1: The required specifications for LNA design.

are presented in Section 3.6. In order to show the versatility of the proposed LNA technique, Section 3.7 presents the measured results of the designed LNA for WCDMA applications.

3.2. Conventional CMOS LNA topologies

3.2.1 Wideband CMOS LNA

Several LNA topologies for wideband have been reported [10-13]. In recent research, these topologies are classified as a shunt feedback common source (CS) type and a common gate (CG) type, presented in Figure 3.2. The shunt feedback CS type is referred as an LNA having feedback resistance, R_F, between a gate and a drain of a MOS transistor for wideband input matching. In contrast, the CG type is defined as an LNA that has an RF input signal injected into a source of a MOS transistor for the same purpose. The input impedance and the voltage gain of the shunt feedback CS type are

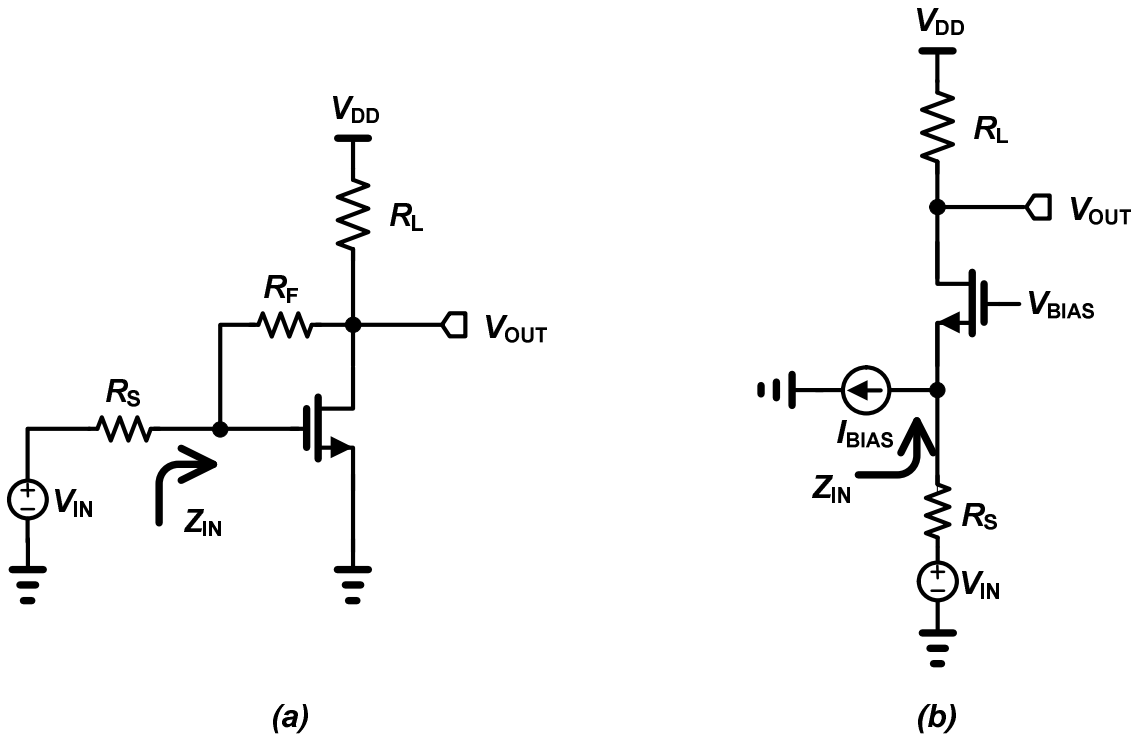


Figure 3.2: Conventional wideband LNA topologies. (a) Shunt feedback common source amplifier. (b) Common gate amplifier.

approximated as the following equations when the output impedance of the MOS transistor is assumed to be infinite for simplicity.

$$Z_{IN} \cong \frac{R_F + R_L}{1 + g_m R_L} \ , \tag{3.1}$$

$$Gain \cong \frac{g_m - 1/R_F}{1/R_L + 1/R_F}, \tag{3.2}$$

where R_L is the load resistance, and g_m is the small-signal trans-conductance of the MOS transistor. From these equations, the shunt feedback CS type amplifier provides good wideband input matching and flat gain because of the absent of frequency-dependent variables in (3.1) and (3.2). However, this topology suffers from poor NF and high power

consumption. From (3.1), the R_F tends to be a few hundred ohms for input matching with the source resistance, R_S, of typically 50 Ω. This restricted R_F value offers gain degradation, as shown in (3.2). In addition, the thermal noise of R_F can contribute to significant noise figure degradation of the LNA. Thus, even for moderate gain and NF performance, the shunt feedback CS LNA needs high power consumption. Furthermore, the linearity of the topology can be poor since the RF signal can flow through relatively large parasitic capacitance, such as the gate-to-drain capacitance, C_{gd}.

The CG type amplifier for wideband is superior in linearity and stability to the shunt feedback CS type LNA due to low parasitic capacitances in the RF signal path. However, the CG type LNA suffers from low gain and high NF, both of which are still inherent problems in the wideband LNA. In the CG LNA, the input impedance is simplified as $1/g_m$ when it operates in low frequency. Thus, the trans-conductance is uniquely defined as 20 mS for 50 Ω input matching and can affect gain and noise performance. The voltage gain of the CG LNA is proportional to g_m and noise factor is inversely proportional to g_m [14]. Due to this restricted g_m value for input matching, the CG LNA provides limited gain and noise performances, which is difficult to adapt to various applications. Thus, for high data-rate applications, the gain and noise performance of conventional LNA topologies need to be enhanced. In addition, the topologies need to reduce power consumption for adapting the mobile terminal efficiently.

3.2.2 CG LNA with positive feedback

To alleviate the restricted g_m value for input matching of the CG LNA, a positive feedback technique has been reported, as shown in Figure 3.3 [15-17]. The shunt-shunt

positive feedback loop senses the output voltage, V_{OUT}, and generates a current to the input at the same phase. The amount of the injected current into the input is approximated as a positive feedback loop gain, A_{POS}, which is a multiplication of the trans-conductance in a positive feedback stage, g_{mPOS}, and load resistance, R_L when transistors are assumed to have infinite output impedance. From a general feedback theory, the input impedance of the circuit with a shunt-shunt positive feedback loop is determined as the open loop input impedance of the CG topology divided by *(1-loop gain)* [18]. Thus, the input impedance of the circuit is given as

$$Z_{IN} = \frac{1}{g_m(1 - A_{POS})}, \tag{3.3}$$

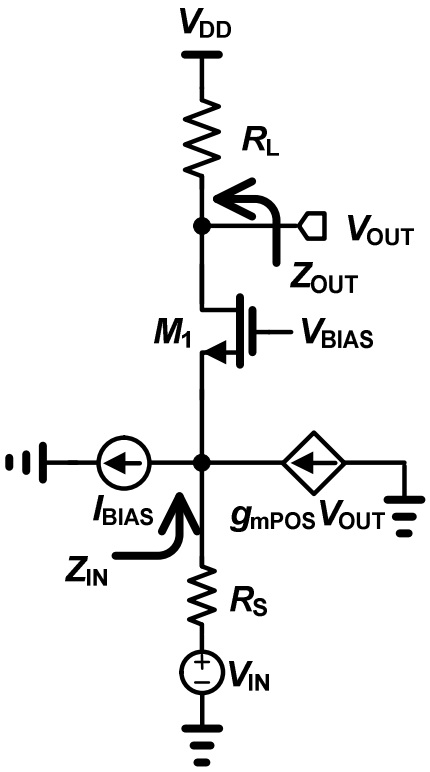


Figure 3.3 : Common gate amplifier with a positive feedback technique.

where g_m is the trans-conductance of the M_1 transistor. Equation (3.3) illustrates that g_m can be higher than 20 mS by increasing the positive loop gain, A_{POS}, while maintaining 50 Ω input matching. Thus, an arbitrary g_m value for input matching is achieved by using this positive feedback technique. On the other hand, the output impedance of the circuit with the shunt-shunt positive feedback is also calculated using the same method as in feedback theory.

$$Z_{OUT} \cong \frac{Z^*_{OUT}}{(1 - A_{POS})}, \tag{3.4}$$

where Z^*_{OUT} is the output impedance without the feedback loop. Equation (3.4) shows that the output impedance can be enlarged as A_{POS} approaches unity. Even though a large value of A_{POS} increases g_m and the output impedance while retaining input matching, the value of A_{POS} should be under unity to prevent oscillation of the circuit.

In this positive feedback topology, the effective trans-conductance, G_M, in the input matching condition, $R_S = Z_{IN}$, is derived as

$$G_M = \frac{Z_{IN}}{Z_{IN} + R_S} g_m = \frac{g_m}{2}. \tag{3.5}$$

From the equation, the G_M of the positive feedback topology has the same formula as that of the CG topology. The voltage gain of the positive feedback topology, which is G_M times the output impedance, can be enhanced when compared to one based on the CG topology due to increased output impedance. In addition, the noise factor can be computed as the following expression when the noise contribution from the load is ignored for simplicity.

$$F = 1 + \frac{\gamma}{\alpha g_m R_S} + F_{Pos.FB.}, \tag{3.6}$$

where γ is the thermal noise coefficient of M_1, α is defined as the ratio of g_m and the zero bias drain conductance g_{d0}. The second term of the right-hand side in (3.6) represents the channel noise contribution of M_1, and the third term, $F_{POS.FB}$, represents the noise introduction of the positive feedback stage. As the positive feedback stage itself also generates noise into the input of the topology, the overall noise factor needs to include this effect, as shown by (3.6). In the expression, the noise factor of the topology is also the same as that of the CG case except for the third term. From both (3.5) and (3.6), with the help of the arbitrary g_m value for the input matching, high voltage gain and low noise can be realized if a high g_m and a high A_{POS} value are chosen in the circuit design. However, the high g_m value imposes high power consumption of the circuit since the bias current of a MOSFET transistor is proportional to g_m. Hence, improved gain and noise figure through the high g_m value cannot be reached without high-power consumption in the positive feedback topology.

3.3. Concept of the low noise wideband LNA

To achieve low power consumption with high gain and low noise simultaneously, a CG LNA with a positive-negative feedback technique is proposed. In this topology, the same positive feedback loop is utilized, and a negative feedback loop having a gain of $-A_{NEG}$ is inserted between the source and the gate of the M_1 transistor, as shown in Figure 3.4. From this configuration, the input impedance is computed from the feedback theory as

$$Z_{IN} = \frac{1}{g_m(1 - A_{POS})} \times \frac{1}{(1 + A_{NEG})}. \tag{3.7}$$

The expression represents the previous input impedance of the positive feedback in (3.3) divided by $(1+A_{NEG})$, where A_{NEG} is the negative feedback loop gain. The dividing term of $(1+A_{NEG})$ is added since the negative feedback is applied by shunt-series feedback as an independent feedback loop having no correlation with the previous positive feedback. From the equation, the proposed positive-negative feedback topology still offers the arbitrary g_m value for input matching. Furthermore, the required g_m value for input matching in the proposed topology can be smaller than the one in the positive feedback case.

Referring again to Figure 3.4, the negative feedback loop senses a small-signal voltage from the source of M_1, v_S, and the feedback loop amplifies v_S with the gain of $-A_{NEG}$. The output voltage of the negative feedback loop, which is expressed as $-A_{NEG}\,v_S$, is seen by

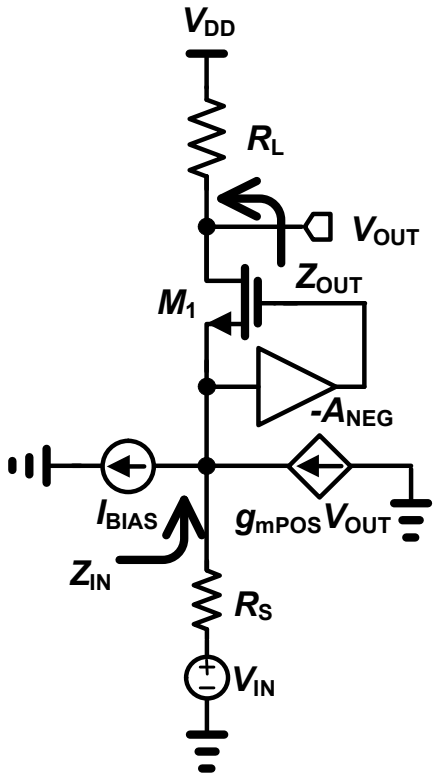


Figure 3.4 : Conceptual diagram of proposed topology.

the gate of M_1. In this case, the small-signal voltage difference between the gate and the source of M_1 can be defined as $(1+A_{NEG})v_S$. Thus, G_M of the topology is calculated as equation (3.8) when input matching is considered.

$$G_M = \frac{Z_{IN}}{Z_{IN}+R_S}(1+A_{NEG})g_m = \frac{g_m}{2}(1+A_{NEG}) \tag{3.8}$$

It is observed that G_M increases by $(1+A_{NEG})$ times in this topology compared to that in the previous positive feedback case. In addition, the output impedance of the proposed topology can be estimated from the feedback theory as well.

$$Z_{OUT} \approx \frac{Z_{OUT}^*}{(1-A_{POS})} \times (1+A_{NEG}) \tag{3.9}$$

The output impedance of the topology also increases by $(1+A_{NEG})$ times compared to that of the positive feedback topology since the shunt-series negative feedback loop is inserted. Therefore, overall gain is enhanced due to the increment of both the effective trans-conductance and the output impedance.

The noise factor of the proposed topology can be expressed as

$$F = 1 + \frac{\gamma}{\alpha g_m R_S (1+A_{NEG})} + F_{Pos.FB.} \tag{3.10}$$

The channel noise of M_1, which is the second term of the right hand side in (3.10), is divided by a $(1+A_{NEG})$ and the noise factor of the positive feedback stage is the same when these are compared to the positive feedback configuration. The boosted G_M due to negative feedback contributes to reducing the channel noise of M_1. Both of these gain and noise enhancements through the positive-negative feedback technique are achieved with a low g_m, which leads to low power consumption. By using the proposed technique, high

gain and low noise with low power as well as the arbitrary g_m value for input matching in the CG configuration are achieved.

3.4. Implementation of the low noise wideband LNA

The conceptual idea of the positive-negative feedback technique is implemented by differential configuration with the CMOS technology in Figure 3.5. The differential structure can reject common mode noise, such as substrate noise, and is suitable for connecting directly with the following stage such as a double-balanced mixer [19].

In the schematic, the positive feedback loop is formed by PMOS transistors that are cross-connected from the output to the input. The gates of PMOS transistors M_{P1} and M_{P2} sense the

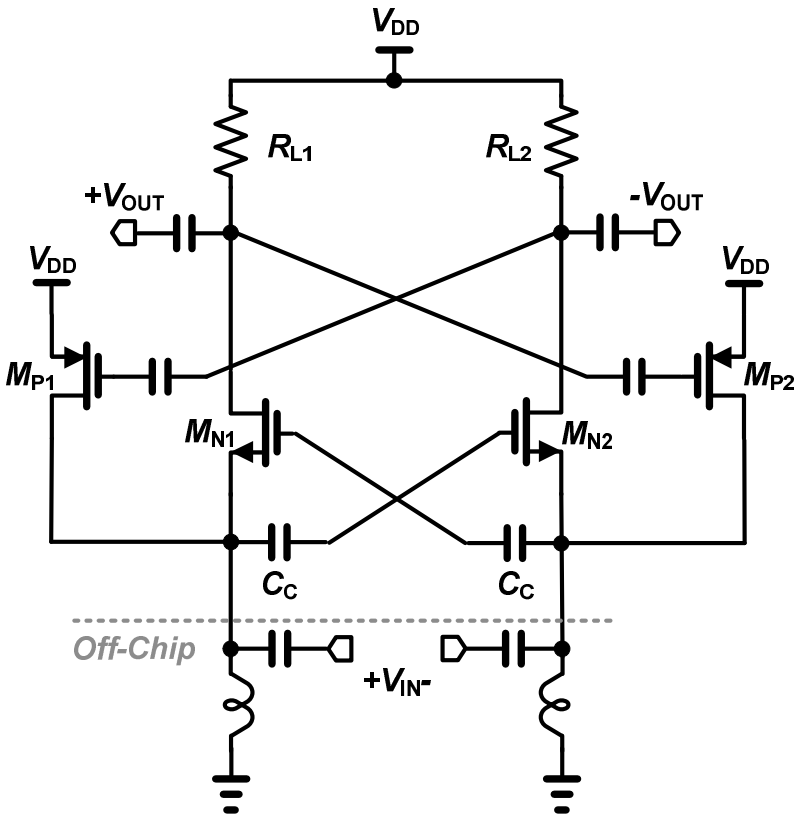


Figure 3.5 : Entire schematic of the proposed topology.

opposite positive output signals, $-V_{OUT}$ and $+V_{OUT}$, and output currents of M_{P1} and M_{P2} inject to input ports $+V_{IN}$ and $-V_{IN}$. The capacitors in front of the gates in PMOS transistors, which are abbreviated for simplicity, are used as DC bias blocking from the output nodes and DC bias receipt from gate biasing circuits. The gate bias and the size of M_{P1} and M_{P2} need to be the same to have a balanced differential signal and be adjusted to have a zero to one loop gain for stable region operation. In addition, the size of M_{P1} and M_{P2} is designed to be as small as possible since the parasitic capacitance of these PMOS transistors can limit the bandwidth of the entire circuit.

The negative feedback loop is implemented by a cross-coupled capacitor, C_C. The differential input signals of the circuit flow to the sources of NMOS transistors, M_{N1} and M_{N2}, and these are cross-coupled to the gates of the opposite NMOS transistors through capacitors. The C_C is made by a metal-to-metal (MIM) capacitor that prevents thermal noise generation in an ideal case. Therefore, the capacitors consisting of the negative feedback loop can be designed to minimize the noise figure of the entire circuit. In addition, the loop gain of the negative feedback needs to be high for maximizing gain and minimizing the noise figure of the topology. In this structure, if the differential signals are perfectly balanced, the negative feedback loop gain, A_{NEG}, is given as $(C_C\text{-}C_{gs})/(C_C+C_{gs})$, in which C_{gs} is the gate-to-source capacitance of M_{N1} or M_{N2}. A_{NEG} can be nearly unity when C_C is much larger than C_{gs}.

3.5. Analysis of the low noise wideband LNA

3.5.1 Gain

The gain-boosting mechanism of the proposed topology due to enlarged G_M and the output impedance is illustrated in Figure 3.6. The diagram represents a single-ended model of an in-phase output signal, $+V_{OUT}$, for simplicity. The gain enhancement of an out-of-phase output signal, $-V_{OUT}$, can be explained using the same methods as well. Basically, the in-phase voltage input signal, $+V_{IN}$, is amplified from the source to the

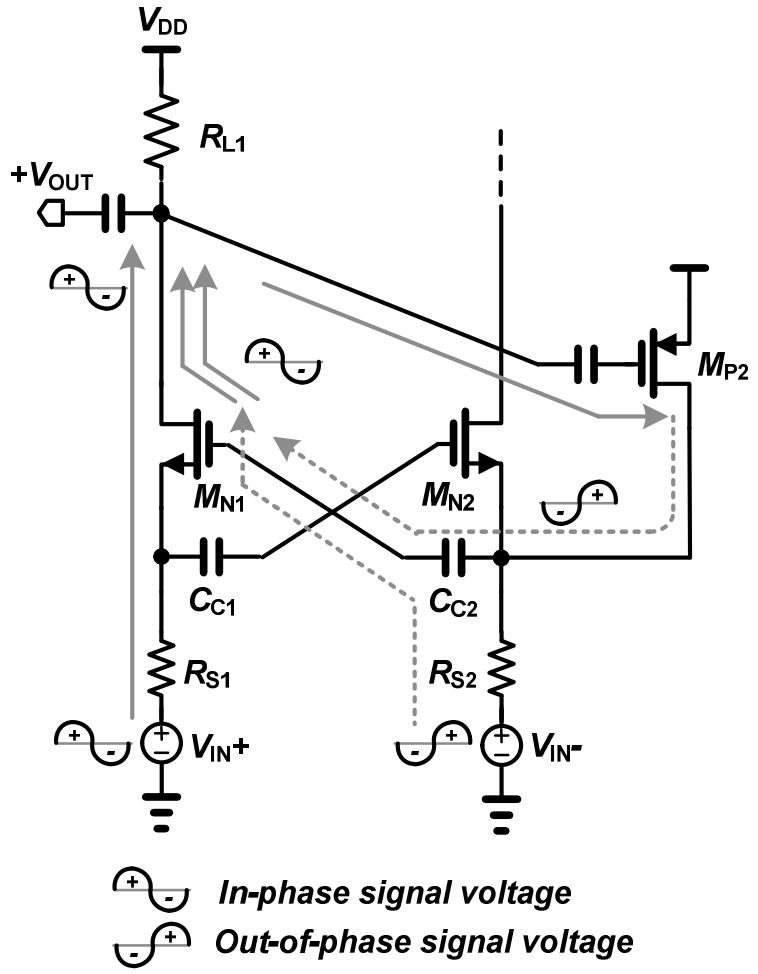


Figure 3.6 : Graphically-explained gain boosting mechanism in a single-ended model.

drain of M_{N1} with the same phase through the trans-conductance of M_{N1} and the load resistor, R_{L1}. In the positive feedback loop, the amplified output voltage, $+V_{OUT}$, is sensed at the gate of M_{P2}, and $+V_{OUT}$ generates the additional out-of-phase voltage signal with a combination of the source resistor, R_{S2}, and the input impedance of M_{N2}. Through the negative feedback loop, out-of phase output voltage signals from M_{P2} and from the input port go through the gate of M_{N1}, and then M_{N1} amplifies these signals as in-phase. Thus, the in-phase input signal into the source of M_{N1}, the out-of-phase signal from M_{P2} into the gate of M_{N1}, and the out-of-phase input signal into the gate of M_{N1} are amplified through M_{N1}. These three amplified voltage signals are

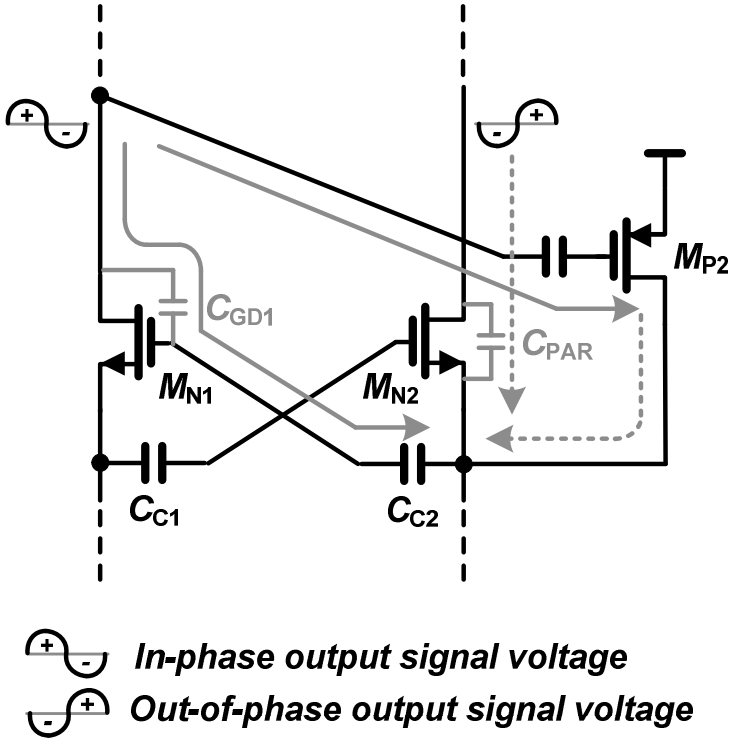


Figure 3.7 : Graphically-explained S12 characteristic in a single-ended model.

combined at the output port as the same phase and these output signals contribute to gain boosting in the proposed topology.

3.5.2 Stability

In such a high-gain LNA design, stability needs to be carefully considered to prevent the circuit from oscillation. Even though the CG type LNA itself is very stable due to small parasitic capacitances between the input and the output port, we still need to investigate the stability issue due to the additional positive feedback loop in the topology. Figure 3.7 represents how much the output signal transfers to input, which corresponds to the reverse isolation s-parameter, S_{12}. When we only consider feedback signals from the output to the input, the in-phase output signal flows to the input by two paths. One path is that the in-phase output voltage signal couples through the gate-to-drain capacitance of M_{N1} and presents in-phase voltage at the input. The other path is that in-phase output voltage changes to out-of phase voltage at the input through the positive feedback loop.

On the other hand, out-of-phase output voltage couples to input as out-of-phase through the source-to-drain capacitance, C_{PAR}, which occurs in routing of layout with a small value. These two out-of-phase voltage paths and an in-phase voltage path can partially cancel out each other at the input port. Due to the cancellation, increased isolation between the input and the output, which means decreased S_{12}, provides higher stability even though we design the circuit with a large device size of M_N and high A_{POS} value for achieving high gain.

3.5.3 Noise figure

Figure 3.8 illustrates the analysis of the noise figure in the proposed topology. In the analysis, the bias current of transistors is assumed to be ideal to simplify the calculation. In addition, only the thermal noise of transistors and resistors is taken into account since the circuit is assumed to operate in low frequency. In this condition, the noise factors contributed by M_N, M_P, and R_L can be derived by the following expressions because the noise factor of each component is given as output noise current from the component over output noise current from the source.

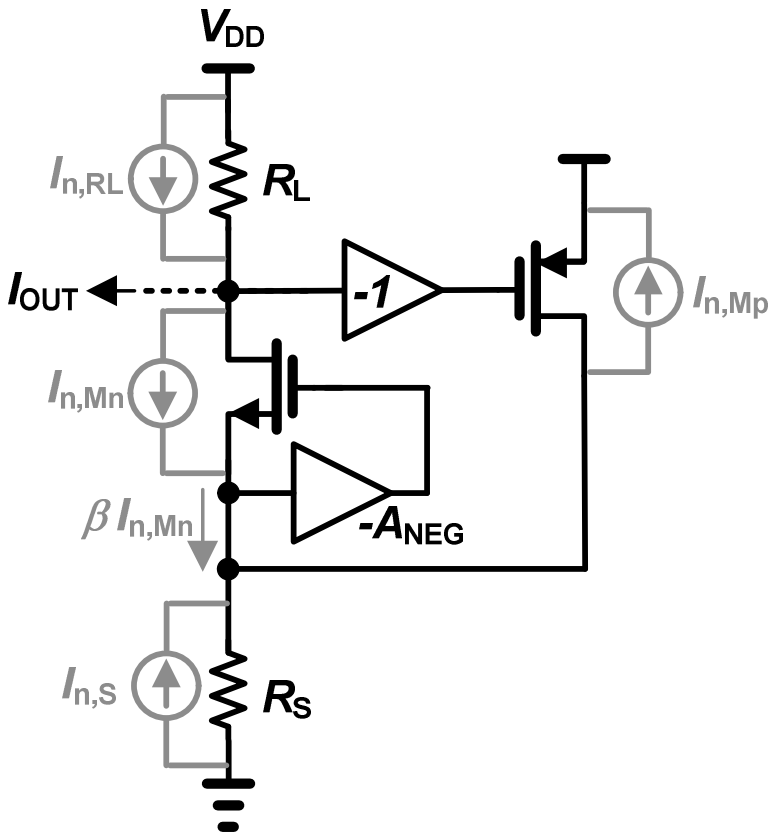


Figure 3.8 : Channel noise contributions of the LNA in simplified single-ended model.

$$F_{Mn} = \frac{(\beta I_{n,Mn})^2}{(\beta I_{n,S} R_S (1 + A_{NEG}) g_m)^2}, \tag{3.11}$$

$$F_{Mp} = \frac{(\beta I_{n,Mp} R_S (1 + A_{NEG}) g_m)^2}{(\beta I_{n,S} R_S (1 + A_{NEG}) g_m)^2}, \tag{3.12}$$

$$F_{RL} = \frac{I_{n,RL}{}^2}{(\beta I_{n,S} R_S (1 + A_{NEG}) g_m)^2}, \tag{3.13}$$

where

$$\beta = \frac{1}{1 + (1 + A_{NEG}) g_m R_S}. \tag{3.14}$$

The output noise from the source, which is given in the denominator of from (3.11) to (3.13), includes boosted g_m, which reduces the noise figure of the topology. In this case, the total noise factor is approximated as

$$F = 1 + \frac{\gamma(1 - A_{POS})}{\alpha(1 + A_{NEG})} + \frac{\gamma}{\alpha} g_{m,Mp} R_S + \frac{R_S}{R_L}(2 - A_{POS})^2. \tag{3.15}$$

This equation comes from the assumption of the input matching condition, $R_S = 1/g_m (1+A_{NEG})(1+A_{POS})$, as shown in (3.7). From the equation, the channel noise of M_N in the second term of the right-hand side in (3.15) can be reduced by the positive feedback loop gain as well as the negative feedback loop gain. As both A_{NEG} and A_{POS} increase, the channel noise of M_N can be greatly decreased. The channel noise due to the PMOS transistor, given in the third term of equation (3.15), can be also decreased by choosing a low g_m value of M_P. Furthermore, the load noise given in the fourth term of (3.15) is also reduced by the positive feedback loop gain.

3.5.4 Linearity

For analyzing the IIP3 of the circuit topology, power series model based on Sansen's theory can be applied to the topology. [20] Although the model is only effective in weekly non-linear memoryless systems, it facilitates the calculations of complicate feedback and differential configurations. For the first step, the positive feedback case of the proposed topology is analyzed separately for simplicity, as shown in Figure 3.9. (a). The non-linear amplifier portions, consisting NMOS transistors of the topology, are characterized by power series coefficients, g_1, g_2, g_3. In addition, the positive feedback loops, forming PMOSs in the topology, have non-linear coefficients, F_1, F_2, F_3. This model for the positive feedback case assumes no mismatch characteristics between the differential paths of the topology. From the assumptions, the differential output signals,

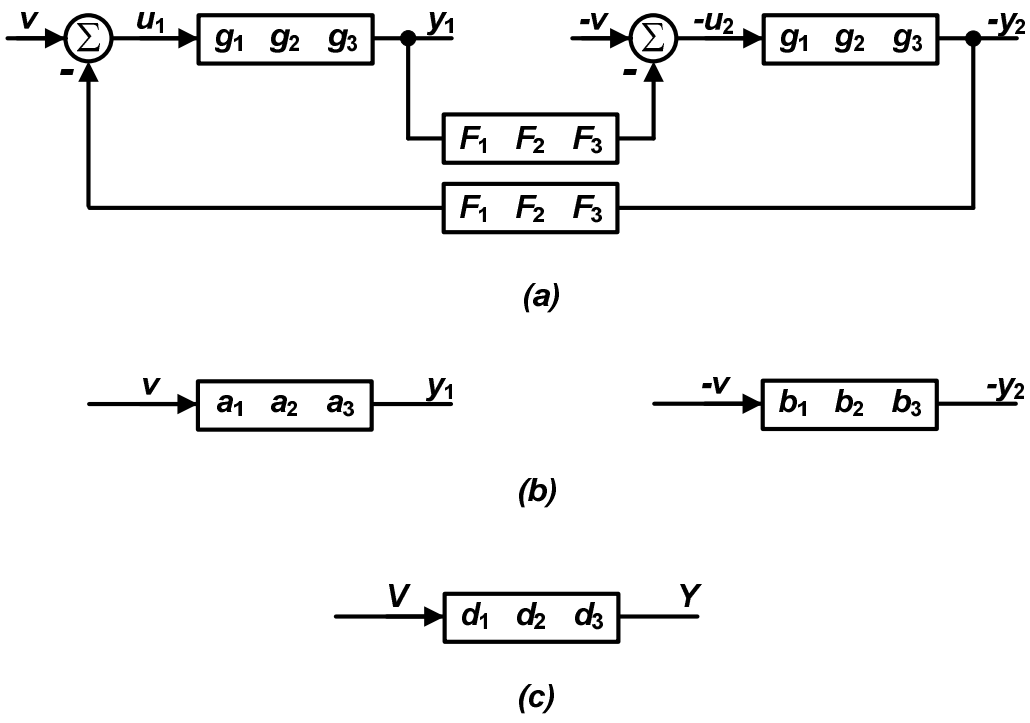


Figure 3.9 : Feedback block diagrams for the positive feedback case.

y_1, $-y_2$, are calculated by differential input signals, v, $-v$, and the feedback coefficients as follows.

$$u_1 = v + F_1 y_2 - F_2 y_2^{\,2} + F_3 y_2^{\,3}, \tag{3.16}$$

$$u_2 = v + F_1 y_1 + F_2 y_1^{\,2} + F_3 y_1^{\,3}, \tag{3.17}$$

$$y_1 = g_1 u_1 + g_2 u_1^{\,2} + g_3 u_1^{\,3}, \tag{3.18}$$

$$y_2 = g_1 u_2 - g_2 u_2^{\,2} + g_3 u_2^{\,3}. \tag{3.19}$$

For further simplifying the diagram, the other model, shown in Figure 3.9 (b), describes differential systems having the same characteristics as the system in Figure 3.9 (a). From this diagram, the positive signal path, which composes of input signal, v, and output signal, y_1, and the negative signal path, which composes of input signal, $-v$, and output signal, $-y_2$, are modeled using non-linear coefficient of $a_1, a_2, a_3,$ and that of b_1, b_2, b_3, respectively. In this case,

$$y_1 = a_1 v + a_2 v^2 + a_3 v^3, \tag{3.20}$$

$$y_2 = b_1 v - b_2 v^2 + b_3 v^3. \tag{3.21}$$

From (3.20) and (3.21), each non-linear coefficient is obtained when the input signal is supposed to approaches to zero, and it is given as

$$\left.\frac{\partial y_1}{\partial v}\right|_{v=0} = a_1, \quad \left.\frac{\partial^2 y_1}{\partial^2 v}\right|_{v=0} = 2a_2, \quad \left.\frac{\partial^3 y_1}{\partial^3 v}\right|_{v=0} = 6a_3, \tag{3.22}$$

$$\left.\frac{\partial y_2}{\partial v}\right|_{v=0} = b_1, \quad \left.\frac{\partial^2 y_2}{\partial^2 v}\right|_{v=0} = -2b_2, \quad \left.\frac{\partial^3 y_2}{\partial^3 v}\right|_{v=0} = 6b_3. \tag{3.23}$$

For finding coefficient a_1, we calculate $\partial u_1 / \partial v$ from (3.16) to (3.19), and then

$$\frac{\partial u_1}{\partial v} = 1 + F_1 \frac{\partial y_2}{\partial v} - 2F_2 y_2 \frac{\partial y_2}{\partial v} + 3F_3 y_2^{\,2} \frac{\partial y_2}{\partial v}, \tag{3.24}$$

where

$$\frac{\partial y_2}{\partial v} = g_1 \frac{\partial u_2}{\partial v} - 2g_2 u_2 \frac{\partial u_2}{\partial v} + 3g_3 {u_2}^2 \frac{\partial u_2}{\partial v}, \tag{3.25}$$

$$\frac{\partial u_2}{\partial v} = 1 + F_1 \frac{\partial y_1}{\partial v} + 2F_2 y_1 \frac{\partial y_1}{\partial v} + 3F_3 {y_1}^2 \frac{\partial y_1}{\partial v}. \tag{3.26}$$

In the initial condition v=0, the output signals y_1 and y_2 approaches to zero from (3.20) and (3.21). In addition, the difference between input and feedback signal u_1 and u_2 approaches to zero from (3.16) and (3.17) as well. Substituting (3.25) and (3.26) into (3.24), we get

$$\left.\frac{\partial u_1}{\partial v}\right|_{v=0} = 1 + F_1 \left.\frac{\partial y_2}{\partial v}\right|_{v=0} = 1 + g_1 F_1 (1 + F_1 \left.\frac{\partial y_1}{\partial v}\right|_{v=0}), \tag{3.27}$$

and according to eq. (3.18)

$$\frac{\partial y_1}{\partial v} = g_1 \frac{\partial u_1}{\partial v} + 2g_2 u_1 \frac{\partial u_1}{\partial v} + 3g_3 {u_1}^2 \frac{\partial u_1}{\partial v}. \tag{3.28}$$

Thus, the coefficient a_1 simplified from (3.22) is derived from eq. (3.27) and (3.28) when v=0,

$$a_1 = \left.\frac{\partial y_1}{\partial v}\right|_{v=0} = g_1 \left.\frac{\partial u_1}{\partial v}\right|_{v=0} = \frac{g_1(1+g_1F_1)}{1-{g_1}^2{F_1}^2} = \frac{g_1}{1-g_1F_1}. \tag{3.29}$$

When we suppose that the positive loop gain, T, is defined as g_1F_1, we get

$$a_1 = \frac{g_1}{1-T}. \tag{3.30}$$

To find coefficient a_2, we calculate $\partial^2 u_1 / \partial^2 v$ from (3.24)

$$\frac{\partial^2 u_1}{\partial^2 v} = F_1 \frac{\partial^2 y_2}{\partial^2 v} - 2F_2 (\frac{\partial y_2}{\partial v})^2 - 2F_2 y_2 \frac{\partial^2 y_2}{\partial^2 v} + 6F_3 y_2 (\frac{\partial y_2}{\partial v})^2 + 3F_3 {y_2}^2 \frac{\partial^2 y_2}{\partial^2 v}, \tag{3.31}$$

where

$$\frac{\partial^2 y_2}{\partial^2 v} = g_1 \frac{\partial^2 u_2}{\partial^2 v} - 2g_2 (\frac{\partial u_2}{\partial v})^2 - 2g_2 u_2 \frac{\partial^2 u_2}{\partial^2 v} + 6g_3 u_2 (\frac{\partial u_2}{\partial v})^2 + 3g_3 {u_2}^2 \frac{\partial^2 u_2}{\partial^2 v}, \tag{3.32}$$

$$\frac{\partial^2 u_2}{\partial^2 v} = F_1 \frac{\partial^2 y_1}{\partial^2 v} + 2F_2 (\frac{\partial y_1}{\partial v})^2 + 2F_2 y_1 \frac{\partial^2 y_1}{\partial^2 v} + 6F_3 y_1 (\frac{\partial y_1}{\partial v})^2 + 3F_3 {y_1}^2 \frac{\partial^2 y_1}{\partial^2 v}. \tag{3.33}$$

In initial condition, v=0, the $\partial^2 u_1 / \partial^2 v$ summaries as

$$\left.\frac{\partial^2 u_1}{\partial^2 v}\right|_{v=0} = F_1 \left.\frac{\partial^2 y_2}{\partial^2 v}\right|_{v=0} - 2F_2 (\left.\frac{\partial y_2}{\partial v}\right|_{v=0})^2 = F_1 \{g_1 \frac{\partial^2 u_2}{\partial^2 v} - 2g_2 (\frac{\partial u_2}{\partial v})^2\} - 2F_2 (\left.\frac{\partial y_2}{\partial v}\right|_{v=0})$$

$$= F_1 [g_1 F_1 \left.\frac{\partial^2 y_1}{\partial^2 v}\right|_{v=0} + 2g_1 F_2 (\left.\frac{\partial y_1}{\partial v}\right|_{v=0})^2 - 2g_2 (1 + F_1 \left.\frac{\partial y_1}{\partial v}\right|_{v=0})^2] - 2F_2 [g_1 (1 + F_1 \left.\frac{\partial y_1}{\partial v}\right|_{v=0})]^2$$

$$= g_1 F_1^2 \left.\frac{\partial^2 y_1}{\partial^2 v}\right|_{v=0} + \frac{2{g_1}^3 F_1 F_2}{(1-T)^2} - \frac{2g_2 F_1}{(1-T)^2} - \frac{2{g_1}^2 F_2}{(1-T)^2}$$

$$= g_1 F_1^2 \left.\frac{\partial^2 y_1}{\partial^2 v}\right|_{v=0} - 2 \times \frac{{g_1}^2 F_2 (1-T) + g_2 F_1}{(1-T)^2}, \tag{3.34}$$

and according to eq. (3.28)

$$\frac{\partial^2 y_1}{\partial^2 v} = g_1 \frac{\partial^2 u_1}{\partial^2 v} + 2g_2 (\frac{\partial u_1}{\partial v})^2 + 2g_2 u_1 \frac{\partial^2 u_1}{\partial^2 v} + 6g_3 u_1 (\frac{\partial u_1}{\partial v})^2 + 3g_3 {u_1}^2 \frac{\partial^2 u_1}{\partial^2 v}. \tag{3.35}$$

Thus, the coefficient a_2 is derived from eq. (3.27), (3.34) and (3.35) when v=0,

$$a_2 = \frac{1}{2} \left.\frac{\partial^2 y_1}{\partial^2 v}\right|_{v=0} = \frac{1}{2} [g_1 \left.\frac{\partial^2 u_1}{\partial^2 v}\right|_{v=0} + 2g_2 (\left.\frac{\partial u_1}{\partial v}\right|_{v=0})^2] = \frac{g_2 - {g_1}^3 F_2}{(1+T)(1-T)^2} \tag{3.36}$$

To solve coefficient a_3, we calculate $\partial^3 u_1 / \partial^3 v$ from eq. (3.31) in initial condition, v=0,

$$\left.\frac{\partial^3 u_1}{\partial^3 v}\right|_{v=0} = F_1 \left.\frac{\partial^3 y_2}{\partial^3 v}\right|_{v=0} - 6F_2 \left.\frac{\partial y_2}{\partial v}\right|_{v=0} \left.\frac{\partial^2 y_2}{\partial^2 v}\right|_{v=0} + 6F_3 (\left.\frac{\partial y_2}{\partial v}\right|_{v=0})^3, \tag{3.37}$$

where

$$\left.\frac{\partial^3 y_2}{\partial^3 v}\right|_{v=0} = g_1 \left.\frac{\partial^3 u_2}{\partial^3 v}\right|_{v=0} - 6g_2 \left.\frac{\partial u_2}{\partial v}\right|_{v=0} \left.\frac{\partial^2 u_2}{\partial^2 v}\right|_{v=0} + 6g_3 (\left.\frac{\partial u_2}{\partial v}\right|_{v=0})^3 \quad , \tag{3.38}$$

$$\left.\frac{\partial^3 u_2}{\partial^3 v}\right|_{v=0} = F_1 \left.\frac{\partial^3 y_1}{\partial^3 v}\right|_{v=0} + 6F_2 \left.\frac{\partial y_1}{\partial v}\right|_{v=0} \left.\frac{\partial^2 y_1}{\partial^2 v}\right|_{v=0} + 6F_3 (\left.\frac{\partial y_1}{\partial v}\right|_{v=0})^3 . \tag{3.39}$$

Substituting (3.39) into (3.38), we get

$$\left.\frac{\partial^3 y_2}{\partial^3 v}\right|_{v=0} = g_1 F_1 \left.\frac{\partial^3 y_1}{\partial^3 v}\right|_{v=0} + 6g_1 F_2 \left.\frac{\partial y_1}{\partial v}\right|_{v=0} \left.\frac{\partial^2 y_1}{\partial^2 v}\right|_{v=0} + 6g_1 F_3 (\left.\frac{\partial y_1}{\partial v}\right|_{v=0})^3$$

$$-6g_2 \frac{1}{1-T}[F_1 \frac{\partial^2 y_1}{\partial^2 v} + 2F_2 (\frac{\partial y_1}{\partial v})^2] + 6g_3 \frac{1}{(1-T)^3}$$

$$= g_1 F_1 \left.\frac{\partial^3 y_1}{\partial^3 v}\right|_{v=0} + 6g_1 F_2 \frac{g_1}{1-T}[\frac{2g_2 - 2g_1^3 F_2}{(1+T)(1-T)^2}] + 6g_1 F_3 (\frac{g_1}{1-T})^3$$

$$-6g_2 \frac{1}{1-T}[F_1 \frac{2g_2 - 2g_1^3 F_2}{(1+T)(1-T)^2} + 2F_2 (\frac{g_1}{1-T})^2] + 6g_3 \frac{1}{(1-T)^3}$$

$$= g_1 F_1 \left.\frac{\partial^3 y_1}{\partial^3 v}\right|_{v=0} + \frac{12g_1^2 g_2 F_2 - 12g_1^5 F_2^2}{(1+T)(1-T)^3} + \frac{6g_1^4 F_3}{(1-T)^3}$$

$$\frac{-12g_2^2 F_1 + 12g_1^3 g_2 F_1 F_2}{(1+T)(1-T)^3} - \frac{12g_1^2 g_2 F_2}{(1-T)^3} + \frac{6g_3}{(1-T)^3}$$

$$= g_1 F_1 \left.\frac{\partial^3 y_1}{\partial^3 v}\right|_{v=0} + \frac{6}{(1+T)(1-T)^3}[2g_1^2 g_2 F_2 - 2g_1^5 F_2^2 + g_1^4 F_3 (1+T)$$

$$-2g_2^2 F_1 + 2g_1^3 g_2 F_1 F_2 - 2g_1^2 g_2 F_2 (1+T) + g_3 (1+T)] . \tag{3.40}$$

Substituting (3.40) into (3.37), we get

$$\left.\frac{\partial^3 u_1}{\partial^3 v}\right|_{v=0} = g_1 F_1^2 \left.\frac{\partial^3 y_1}{\partial^3 v}\right|_{v=0} + \frac{6F_1}{(1+T)(1-T)^3}[2g_1^2 g_2 F_2 - 2g_1^5 F_2^2 + g_1^4 F_3 (1+T)$$

$$-2g_2^2 F_1 + 2g_1^3 g_2 F_1 F_2 - 2g_1^2 g_2 F_2 (1+T) + g_3 (1+T)]$$

$$-6F_2\frac{\partial y_2}{\partial v}\bigg|_{v=0}\frac{\partial^2 y_2}{\partial^2 v}\bigg|_{v=0}+6F_3(\frac{\partial y_2}{\partial v}\bigg|_{v=0})^3.$$

(3.41)

Reminding,

$$\frac{\partial y_2}{\partial v}=g_1[1+F_1\frac{\partial y_1}{\partial v}]=g_1[1+F_1\frac{g_1}{(1-T)}]=\frac{g_1}{(1-T)},\tag{3.42}$$

$$\frac{\partial^2 y_2}{\partial^2 v}=g_1\frac{\partial^2 u_2}{\partial^2 v}-2g_2(\frac{\partial u_2}{\partial v})^2=\frac{2g_1g_2F_1-2g_1^4F_1F_2+2g_1^3F_2(1+T)-2g_2(1+T)}{(1+T)(1-T)^2}.\tag{3.43}$$

Thus,

$$\begin{aligned}\frac{\partial^3 u_1}{\partial^3 v}\bigg|_{v=0}&=g_1F_1^2\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}+\frac{6}{(1+T)(1-T)^3}[2g_1^2g_2F_1F_2-2g_1^5F_1F_2^2+g_1^4F_1F_3(1+T)\\&\quad-2g_2^2F_1^2+2g_1^3g_2F_1^2F_2-2g_1^2g_2F_1F_2(1+T)+g_3F_1(1+T)]\\&\quad-2g_1^2g_2F_1F_2+2g_1^5F_1F_2^2-2g_1^4F_2^2(1+T)+2g_1g_2F_2(1+T)+g_1^3F_3(1+T)]\\&=g_1F_1^2\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}+\frac{6}{(1+T)(1-T)^3}[g_1^4F_1F_3(1+T)\\&\quad-2g_2^2F_1^2+2g_1^3g_2F_1^2F_2-2g_1^2g_2F_1F_2(1+T)+g_3F_1(1+T)]\\&\quad-2g_1^4F_2^2(1+T)+2g_1g_2F_2(1+T)+g_1^3F_3(1+T)],\end{aligned}\tag{3.44}$$

and according to (3.35)

$$\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}=g_1\frac{\partial^3 u_1}{\partial^3 v}\bigg|_{v=0}+6g_2\frac{\partial u_1}{\partial v}\bigg|_{v=0}\frac{\partial^2 u_1}{\partial^2 v}\bigg|_{v=0}+6g_3(\frac{\partial u_1}{\partial v}_{v=0})^3,\tag{3.45}$$

where

$$6g_2\frac{\partial u_1}{\partial v}\bigg|_{v=0}\frac{\partial^2 u_1}{\partial^2 v}\bigg|_{v=0}+6g_3(\frac{\partial u_1}{\partial v}_{v=0})^3=\frac{6g_2}{1-T}[g_1F_1^2\frac{\partial^2 y_1}{\partial^2 v}\bigg|_{v=0}-2\times\frac{g_1{}^2F_2(1-T)+g_2F_1}{(1-T)^2}]+\frac{6g_3}{(1-T)^3}$$

$$=\frac{12g_1g_2{}^2F_1^2-12g_1{}^4g_2F_1^2F_2-12g_1{}^2g_2F_2(1-T)(1+T)-12g_2{}^2F_1(1+T)+6g_3(1+T)}{(1+T)(1-T)^3}.$$

(3.46)

Thus,

$$\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}=g_1{}^2F_1^2\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}+\frac{6}{(1+T)(1-T)^3}[g_1{}^5F_1F_3(1+T)$$

$$-2g_1g_2{}^2F_1^2+2g_1{}^4g_2F_1^2F_2-2g_1{}^3g_2F_1F_2(1+T)+g_1g_3F_1(1+T)$$

$$-2g_1{}^5F_2{}^2(1+T)+2g_1{}^2g_2F_2(1+T)+g_1{}^4F_3(1+T)$$

$$+2g_1g_2{}^2F_1^2-2g_1{}^4g_2F_1^2F_2-2g_1{}^2g_2F_2(1-T)(1+T)-2g_2{}^2F_1(1+T)+g_3(1+T)] \quad (3.47)$$

$$\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}=g_1{}^2F_1^2\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}+\frac{6}{(1+T)(1-T)^3}[g_1{}^4F_3(1+T)^2+g_3(1+T)^2$$

$$-2g_1{}^5F_2{}^2(1+T)\ -2g_2{}^2F_1(1+T)], \quad (3.48)$$

and

$$\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}=\frac{6}{(1+T)(1-T)^4}[g_1{}^4F_3(1+T)+g_3(1+T)-2g_1{}^5F_2{}^2-2g_2{}^2F_1]. \quad (3.49)$$

Thus, the coefficient a_3 is calculated when v=0,

$$a_3=\frac{1}{6}\frac{\partial^3 y_1}{\partial^3 v}\bigg|_{v=0}=\frac{1}{(1+T)(1-T)^4}[(g_1{}^4F_3+g_3)(1+T)-2(g_1{}^5F_2{}^2+g_2{}^2F_1)]. \quad (3.50)$$

In addition, the non-linear coefficients of b_1, b_2, b_3 can be derived the same method as that of a_1, a_2, a_3 cases. Thus,

$$b_1 = \frac{g_1}{1-T}, \tag{3.51}$$

$$b_2 = \frac{g_2 - g_1^3 F_2}{(1+T)(1-T)^2}, \tag{3.52}$$

$$b_3 = \frac{1}{(1+T)(1-T)^4}[(g_1^4 F_3 + g_3)(1+T) - 2(g_1^5 F_2^2 + g_2^2 F_1)]. \tag{3.53}$$

Finally, the differential non-linear coefficients of a_1 to a_3 and b_1 to b_3 can be simplified as a single-ended model having the non-linear coefficient of d_1, d_2, d_3, shown Figure 3.9 (c). When we suppose input signal, *V,* as $[v-(-v)]/2$ and output signal, *Y,* as $[y_1-(-y_2)]/2$, we can derived the coefficient of d_1, d_2, d_3 from (3.20) and (3.21)

$$d_1 = \frac{g_1}{1-T} \tag{3.54}$$

$$d_2 = 0 \tag{3.55}$$

$$d_3 = \frac{1}{(1+T)(1-T)^4}[(g_1^4 F_3 + g_3)(1+T) - 2(g_1^5 F_2^2 + g_2^2 F_1)] \tag{3.56}$$

From these results, it can be concluded that second order harmonics of the positive feedback configurations is canceled out. It is because that the differential benefits of the LNA are not disappeared even with the positive feedback loop. In addition, the third order term, d_3, can be reduced by choosing proper value of the positive feedback loop gain. These results imply that the design of the proposed LNA has a freedom to choose the IIP3. By adjusting gate biases of M_{P1} and M_{P2}, the IIP3 of the LNA can be greatly increased. These characteristics of the proposed LNA are verified by the simulation results shown in Figure 3.10. The optimal value of IIP3 can be achieved in a certain transconductance of PMOS devices from the LNA. To achieve the accurate biasing of the PMOS devices, bandgap references need to be used for commercial applications.

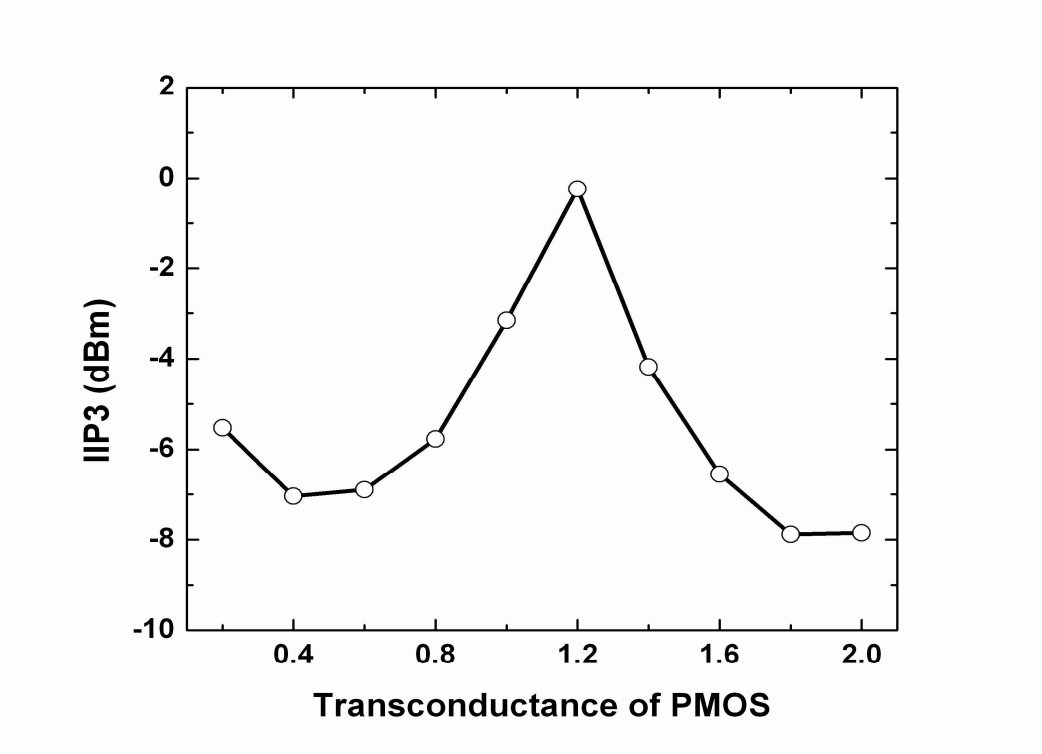


Figure 3.10 : Simulation results of IIP3 with various transconductances of PMOSs.

3.5.5 Output impedance

The output impedance analysis of the proposed LNA is presented in this section. For simplicity, the previous output impedance calculations in the section 3.3 assume no loading effect. Therefore, when we consider the loading effect for more precise calculations, the output impedance can be modeled shown in the Figure 3.11. In this case, the output impedance is derived from output voltage over output current from below two equations in circuit analyses,

$$V_X = (g_{mp}V_{OUT} - g_m V_X - \frac{V_X - V_{OUT}}{r_{ds}})R_S \quad (3.57)$$

,

$$I_{OUT} = -g_m V_X + \frac{V_{OUT}}{R_L} + \frac{V_{OUT} - V_X}{r_{ds}} \quad (3.58)$$

.

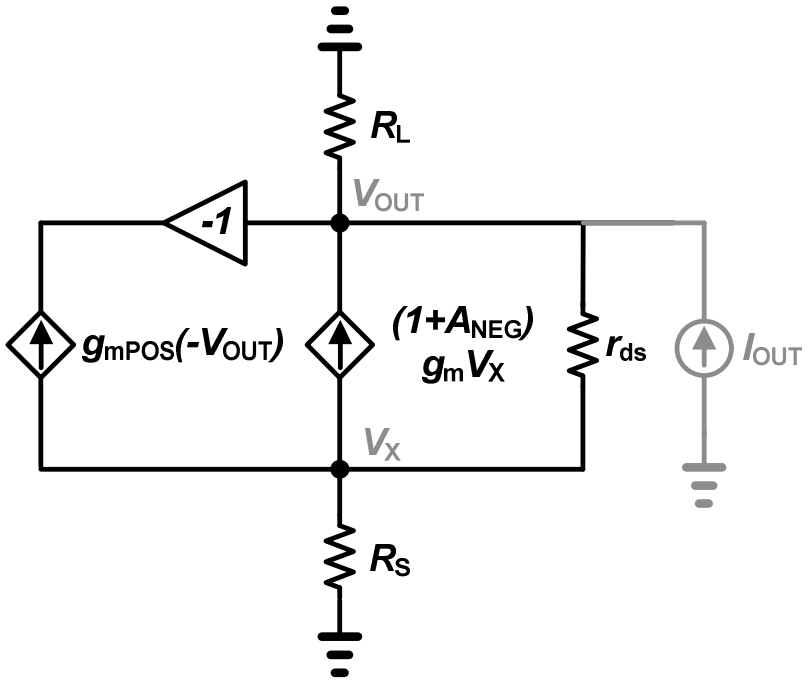


Figure 3.11 : Small signal circuit model in a single side for output impedance calculation.

From these calculations, the output impedance equation of positive feedback only case is

$$Z_{OUT} = \frac{R_L[r_{ds} + R_S(1 + g_m r_{ds})]}{R_L + r_{ds} + R_S(1 + g_m r_{ds})(1 - \alpha_{POS})}, \tag{3.59}$$

and that of the proposed positive-negative feedback case is

$$Z_{OUT} = \frac{R_L[r_{ds} + R_S\{1 + (1 + \alpha_{NEG})g_m r_{ds}\}]}{R_L + r_{ds} + R_S\{1 + (1 + \alpha_{NEG})g_m r_{ds}\}(1 - \alpha_{POS})}. \tag{3.60}$$

For the positive feedback only case, the output impedance increases as the positive feedback loop gain increases from the equation. For the proposed positive-negative feedback case, as we can see, the output impedance increases as the positive feedback loop gain increases and the magnitude of the increment is much higher than positive feedback only case due to the negative feedback loop gain.

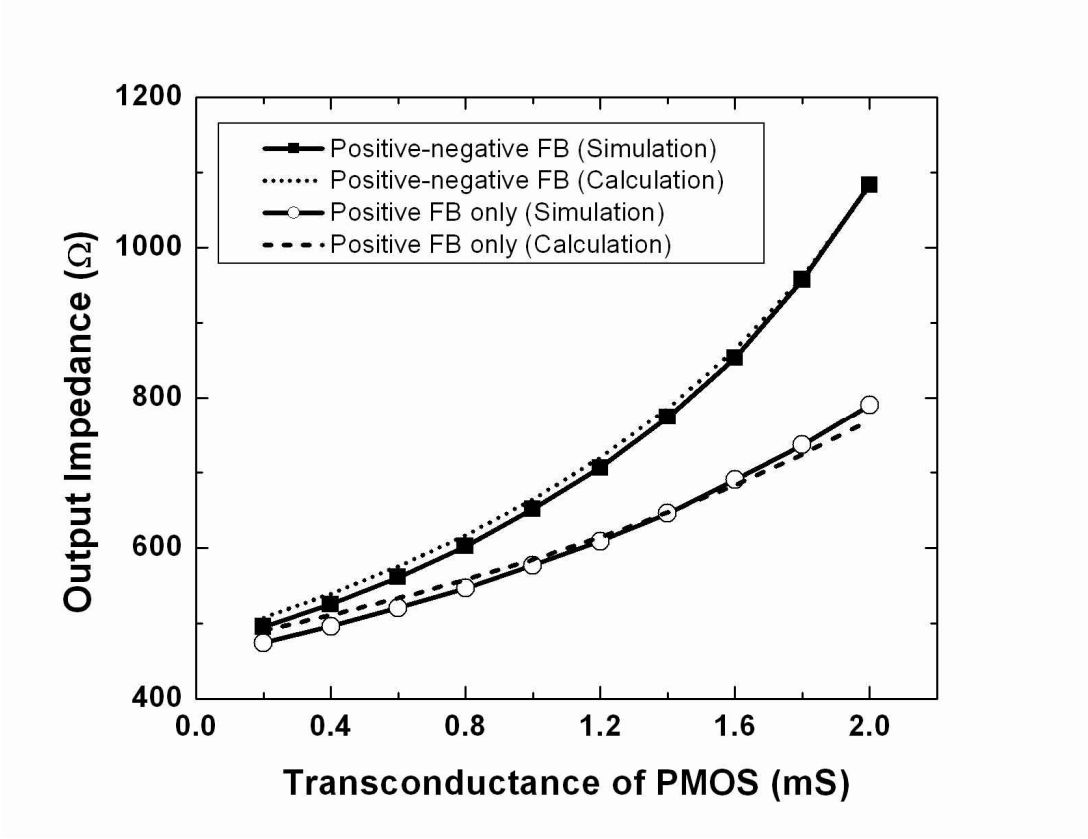


Figure 3.12 : Simulation and calculation results of the output impedance.

This analysis can be verified by simulations shown in Figure 3.12. The horizontal axis shows the output impedance of the LNA and the vertical axis represents positive feedback loop gain. The results shows that the analysis are well matched with simulation results. In addition, the output impedance can be greatly increased through the proposed positive-negative feedback technique.

3.5.6 Comparison with previous feedback technique

From the analyses discussed so far, characteristics of the proposed LNA can be compared with other LNA topologies, such as negative feedback and positive feedback technique itself, as shown in Table 1. It is supposed that negative feedback loop gain is unity and positive feedback loop gain is 0.5 for fair comparison. Through the proposed

topology, we can find out that channel noise of M_N is reduced by half and voltage gain is increased by more than twice when compared to previous topologies in theory.

3.6. Experimental results

A prototype of the proposed LNA was fabricated in 0.18-μm TSMC CMOS technology and assembled in chip-on-board. Figure 3.13 shows the die photo for the LNA. The total chip occupies 0.33 mm^2 including pads and output buffers. The differential output port uses two on-chip buffers designed by source follower configuration with current sources. These buffers offer to match 50 Ω output impedance of measurement equipment and facilitate to measure voltage gain of the LNA. In addition, the output buffers needs to be designed with consideration of linearity in the LNA for valid measurement. The application of the designed LNA is for cognitive radio systems in UHF white space (300 MHz to 698 MHz) and for 4G mobile wireless communications (698 MHz to 862 MHz). The differential LNA is biased at 2mA from a 1.8V supply voltage.

The voltage gain and S-parameters of the LNA are measured using a 4-port network analyzer. Figure 3.14 represents measured the voltage gain, the input return loss, S_{11}, and the reverse transmission, S_{12}. The voltage gain curve is presented when the output buffers and PCB losses are de-embeded. The fabricated LNA is achieved S_{11} lower than -10 dB from 300 MHz to 1.32 GHz, and then the measured 3 dB bandwidth is achieved from 300 MHz to 920 MHz with the input matching condition. The maximum voltage gain measured 21 dB at 430 MHz with 3.8-mW power consumption. The S_{22} and S_{12} are displayed with the effect of buffers included. The S_{22} shows 50 Ω output matching of the buffer, and S_{12} shows over 40 dB reverse isolation in operating frequency.

Table 1 : Comparison characteristics

	Negative feedback	Positive feedback	This work
Z_{IN}	$1/2g_m$	$2/g_m$	$1/g_m$
g_m for input matching	10mS	40mS	20mS
G_M	g_m (=10mS)	$g_m/2$ (=20mS)	$\boldsymbol{g_m}$ (=20mS)
Noise Factor	$1+\frac{\gamma}{2\alpha}+\frac{4R_S}{R_L}$	$1+\frac{\gamma}{2\alpha}+g_{mMp}R_S\frac{\gamma}{\alpha}+\frac{2.25R_S}{R_L}$	$1+\frac{\gamma}{\mathbf{4}\alpha}+g_{mMp}R_S\frac{\gamma}{\alpha}+\frac{2.25R_S}{R_L}$

$A_{NEG}=1,\ A_{POS}=0.5$ *are assumed*

Z^*_{OUT} *output impedance without feedback*

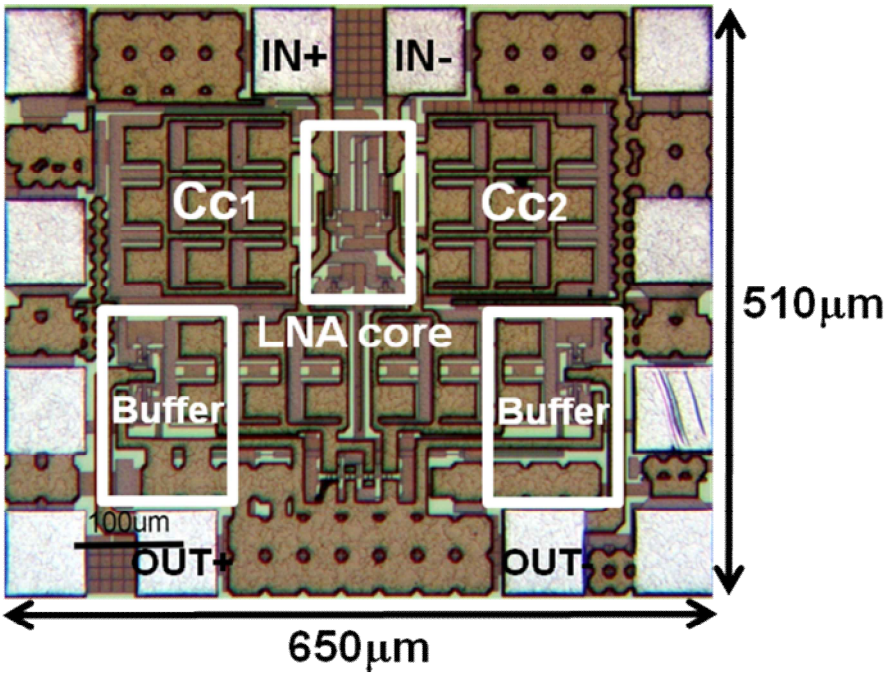


Figure 3.13 : Die micrograph.

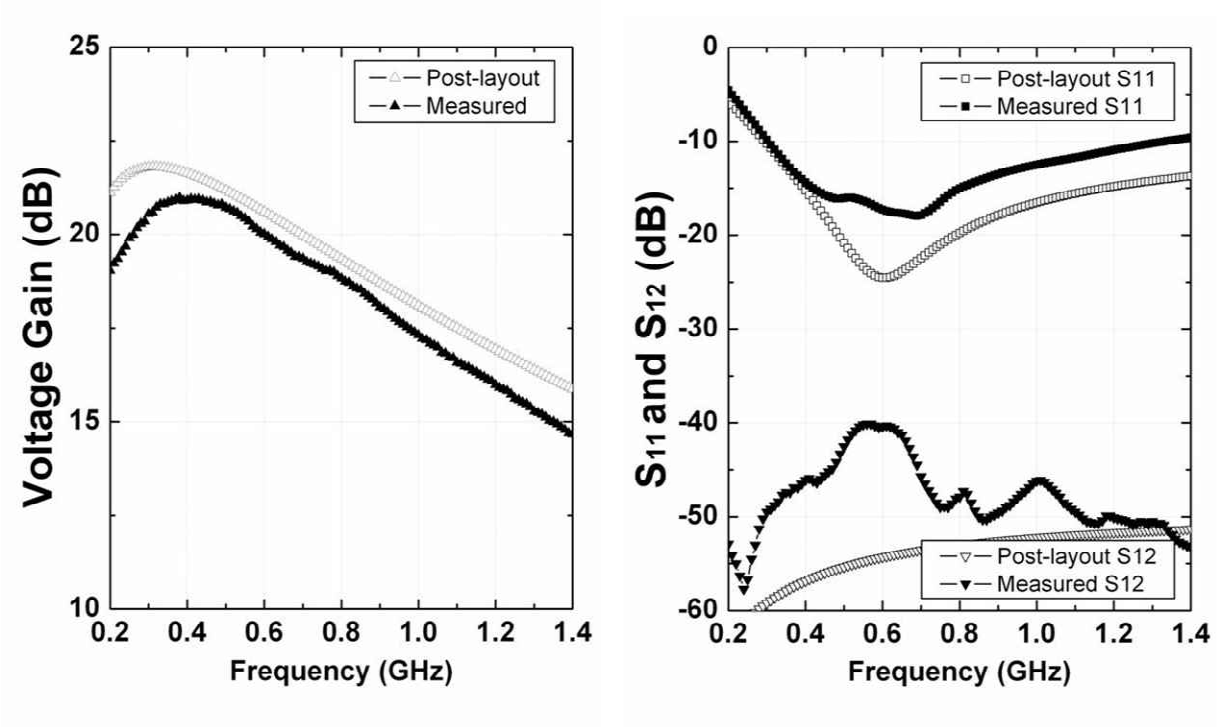


Figure 3.14 : Simulated and Measured voltage gain and S-parameters

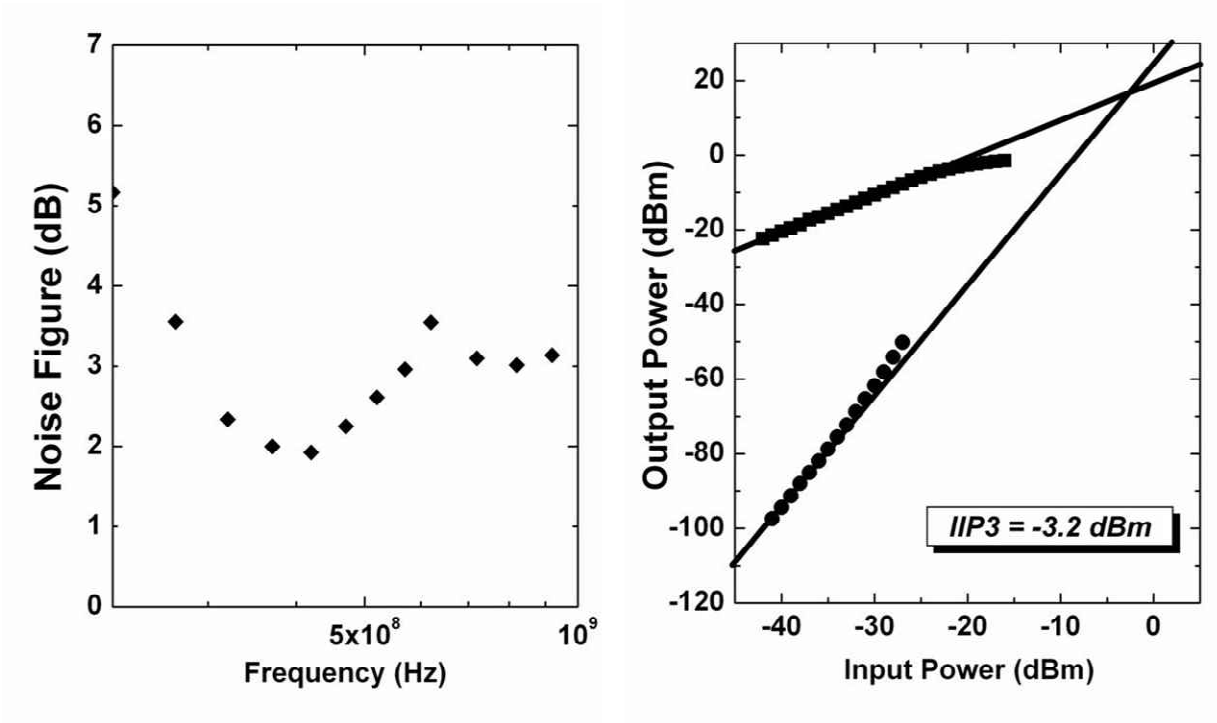


Figure 3.15 : Measured NF and IIP3.

Table 2 : Performance comparison.

Source	Tech-Nology	Freq (GHz)	Gain (dB)	NFmin (dB)	IIP3 (dBm)	Power (mW)	Vdd (V)	Diff-rential?	Total Area (mm^2)
This work	0.18μm	0.3-0.92	**21***	**2**	-3.2	**3.6**	1.8	Yes	**0.33**
[Song] MWCL 2008	0.18μm	0.02-1.18	20.5	3.3	2.7	32.4	1.8	Yes	0.12***
[Wang] JSSC 2006	0.13μm	0.1-0.93	13*	3.6	-7.1**	0.72	1.2	Yes	0.27***
[Blaakmeer] JSSC 2008	65nm	0.2-5.2	15.6*	2.9**	3.5**	14	1.2	Yes	0.75
[Chen] JSSC 2008	0.13μm	0.8-2.1	14.5	2.6	16	17.4	1.5	No	0.66
[Ramzan] ISSCC 2007	0.13μm	1-7	17*	2.4	-4.1	25	1.4	Yes	0.02***
[Borremans] ISSCC 2007	90nm	0-6	17.4	2.5	-8**	9.8	1	No	0.002 ***

** Voltage gain, ** Graphically estimated ,*** Active area size*

The measured NF and IIP3 of the LNA illustrate in Figure 3.15. These performances are measured using external single to differential baluns, and these baluns effect is de-embeded as well. The average noise figure measures 2.8 dB within the operating bandwidth and minimum noise figure value, 2 dB, occurred at the maximum gain frequency. In addition, the measured IIP3 versus frequency is shown in Figure 3.15 (b). It shows IIP3 of -3.2 dBm when applied two-tone at 699 MHz and 700 MHz. In Table 2, the measured result is compared with previously-reported results. The power consumption of this design is less than half of others with an enhanced gain and NF while considering differential topology.

3.7. Experimental results for WCDMA applications

The proposed positive-negative feedback technique is not only applicable to wideband LNA. The technique can be used in specific applications of the LNA, which operate in narrow bandwidth and high frequency. To verify this, the WCDMA LNA is also designed by using the proposed positive-negative feedback technique. In this case, the load resistor needs to be changed to load inductor to have high impedance in high frequency narrow bandwidth, shown in Figure 3. 16. The positive-negative feedback technique requires the differential configuration. Thus, the balun in the input port of the circuits is demanded for converting from single Antenna output port to differential input of the LNA. As this balun has insertion loss, it can be expect that the overall noise figure of the RF system is degraded. Fortunately, the band selection filter between an antenna and a LNA, which is used in mandatory for out-of-band rejection, can offer single-to-differential conversion as well. By using the filter, additional increased noise figure of the system according to single-to-differential conversion could be ignored.

The LNA for WCDMA application is also fabricated in 0.18-μm TSMC CMOS technology and assembled in chip-on-board with the band pass filter. The die photo of the LNA is shown in Figure 3.17. The differential output port uses two on-chip buffers designed by common-source with inductive peaking load to match 50 Ω output impedance of measurement equipment. The operation frequency of the designed LNA is from 2.11GHz to 2.17GHz, which is the frequency for the receiver path of WCDMA. For input band selection filter, the EFCH2140TCA1 from Panasonic is used. The filter

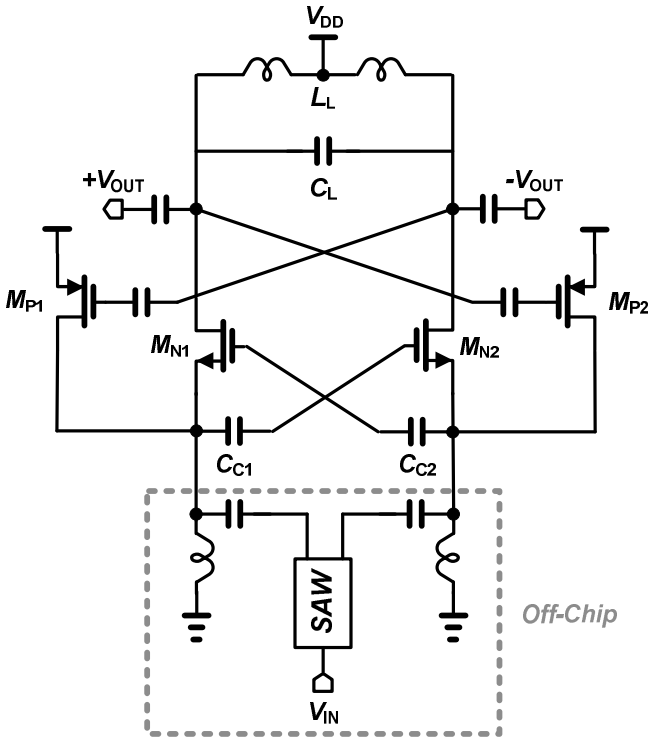


Figure 3.16 : Entire schematic of the WCDMA topology.

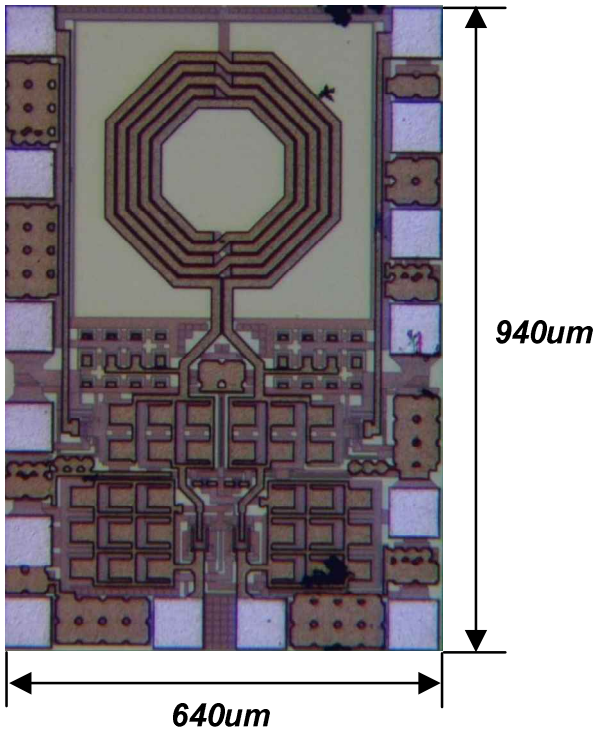


Figure 3.17 : Die photo for WCDMA topology.

provides around 2dB insertion loss in wanted bandwidth with 50-to-100 Ω impedance conversion. The differential LNA is biased at 1.53mA from a 1.8V supply voltage.

In the Figure 3.18, the S-parameters and voltage gain of the LNA are represented. The input return loss is under -10dB in operating frequency, implying input matching condition. In addition, the maximum voltage gain is 23.9dB when the loss of the PCB is extracted. The LNA itself produces 25.9dB voltage gain because the in-band insertion loss of the SAW filter is 2dB. The From Figure 3.19, the IIP3 is measured at -3.7dBm. In addition, noise figure is measured on 1.8dB. The performance of the WCDMA is superior to wideband LNA case. From these results, this research concludes that the positive-negative technique can be applied in wideband LNA as well as a narrow band LNA.

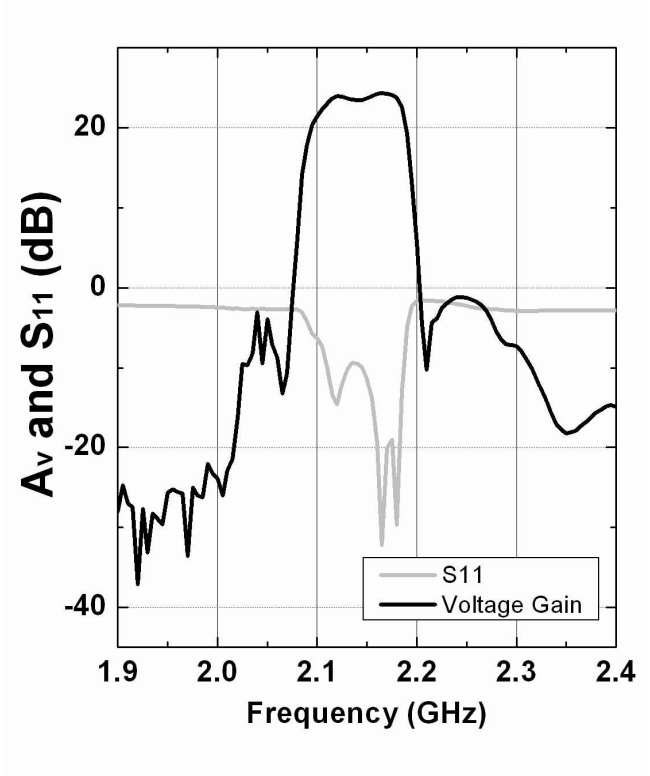


Figure 3.18 : S-parameters and voltage gain for WCDMA topology.

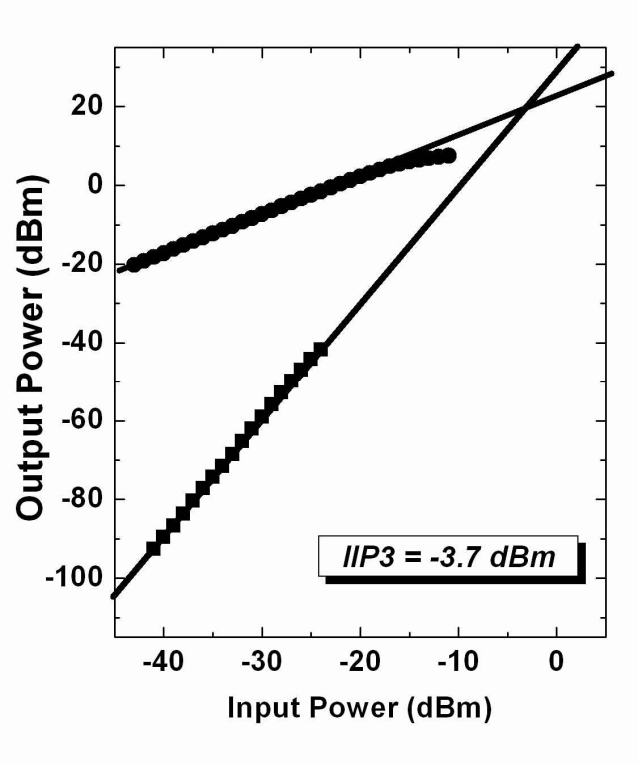


Figure 3.19 : IIP3 for WCDMA topology.

3.8. Conclusions

To achieve high gain and low NF without sacrificing wideband, linearity, and current consumption, a differential g_m boosted CG LNA with the positive-negative feedback technique is proposed. The implemented LNA delivers a maximum voltage gain of 21 dB, a minimum NF of 2 dB, an IIP3 of -3.2 dBm, and 3.6 mW power consumption in 300 to 920 MHz 3 dB S_{21} bandwidth with input matching (S_{11}<-10dB).

IV. SYSTEMATIC ANALYSIS OF FLICKER NOISE

From previous researches, the design of the low noise wideband LNA with high gain and low power is accomplished through the positive-negative feedback technique. The overall RF system noise figure can be enhanced through the LNA. However, flicker noise still needs to be considered for low noise RF receiver since the flicker noise contributes to low frequency noise. In this section, the flicker noise effect is investigated through the system level analysis. By proposing a new flicker noise model and simulating it within an orthogonal frequency-division multiplexing (OFDM) PHY layer, this researcher observed the effect of flicker noise in OFDM systems for the first time. To present this effect, this researcher examined bit error rate (BER) performance with flicker noise by generating raw and channel-coded data. The proposed flicker noise model offers more precise results for OFDM systems since the effect of flicker noise on each subcarrier is included.

4.1. Introduction

Modern wireless communication standards adopt orthogonal frequency-division multiplexing as a modulation scheme due to its robustness against multi-path fading. Orthogonal frequency-division multiplexing divides the wideband signal into many slowly modulated narrowband subcarriers; each of which is exposed to flat fading rather than frequency-selective fading. Additionally, inter-symbol interferences, according to multi-path fading, are avoided by introducing a guard interval between OFDM symbols. In a given bandwidth of the standards, a large fast-fourier transform (FFT) size is more

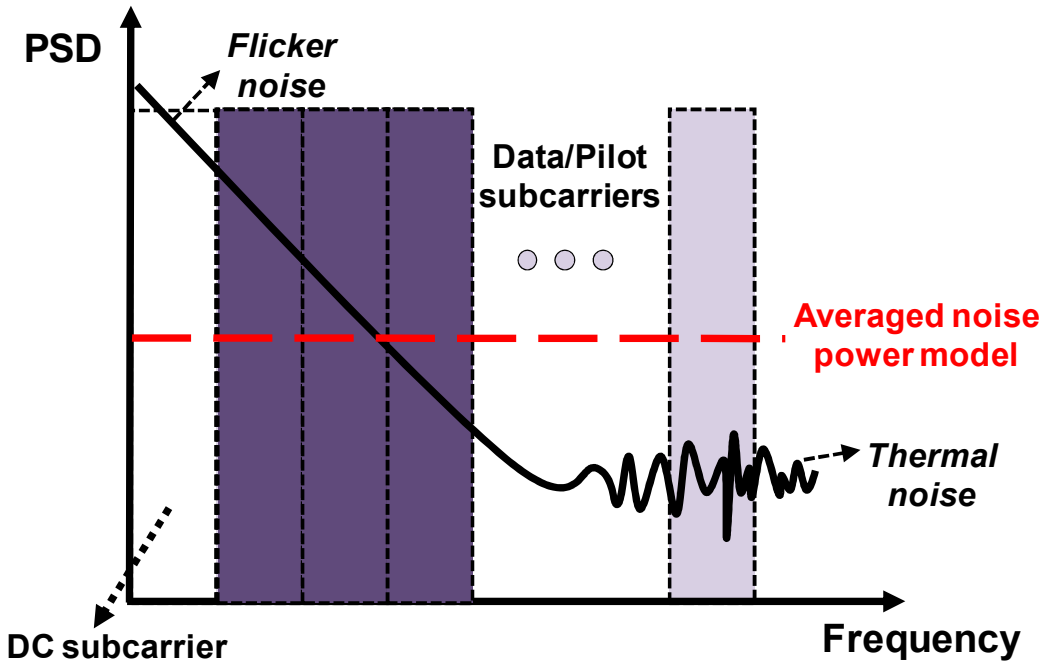


Figure 4.1 : Conventional average noise power model in an OFDM scheme.

effective because it is less susceptible to multipath delay spread. Although the large FFT size reduces subcarrier spacing, most wireless communications standards allocate only one DC subcarrier, which has no information for removing DC offset [21, 22].

Due to reduced subcarrier spacing and only one DC subcarrier allocation, many data subcarriers near DC in OFDM systems are more vulnerable to flicker noise [23]. However, conventional systematic flicker noise analyses, which calculate and simulate averaged noise power in a given bandwidth, result in only signal-to-noise ratio (SNR) degradation over the bandwidth, shown in Figure 4.1 [24, 25]. Thus, existing analyses may not be applicable to OFDM systems because they do not include the effect of flicker noise on each subcarrier. To overcome this restriction, the current work presents a proposed noise model for measuring performance degradation, due to flicker noise, in OFDM PHY layer systems. For the purposes of reducing the effect of noise on these

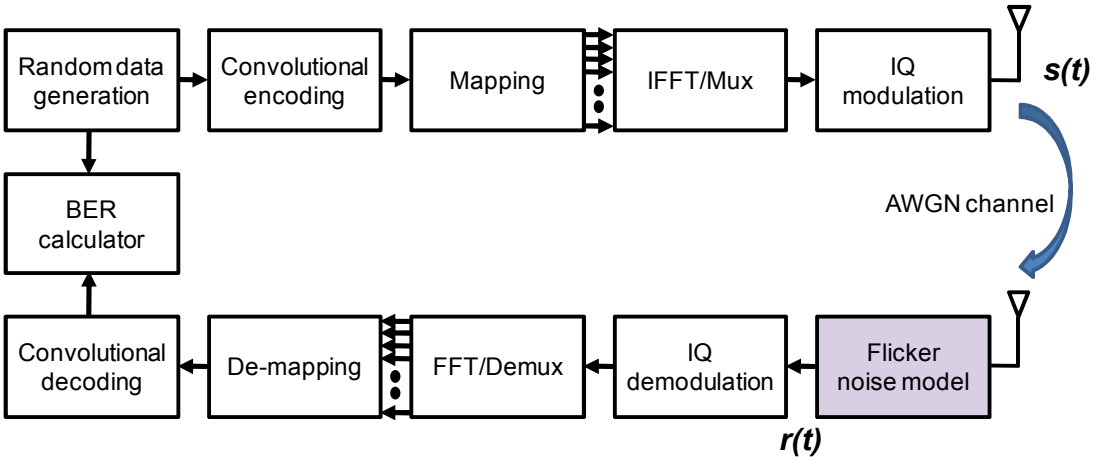


Figure 4.2 : A simplified system model for simulations.

systems, this researcher also tested performance with a channel-coding scheme.

4.2. System models

4.2.1 OFDM system model

Orthogonal frequency-division multiplexing-based baseband processing unit and RF flicker noise circuitry were modeled using MATLAB™. The overall system consisted of a baseband OFDM modem, an I/Q modulator, and a flicker noise block, shown in Figure 4.2. The bit error rate (BER) calculator was inserted between a transmitter (Tx) and a receiver (Rx) for constructing a communication link. The 1024-point IFFT/FFT blocks, with a 10 MHz sampling frequency including 1023 data subcarriers and one DC subcarrier, are spaced at an interval of 9.7656 kHz and placed in the transmitter and receiver paths for the purpose of OFDM modulation.

The 64-QAM mapper/demapper, with a gray code, was used for high data rate transmission. The IFFT/FFT and mapper/demapper size were chosen from required

FFT size	1024	Mapping	64 QAM
Sampling freq.	10 MHz	DC subcarrier	1
Subcarrier spacing	9.765 MHz	Num. of OFDM symbol	200

Figure 4.3 : System specifications for simulations.

specifications of modern communication systems such as IEEE 802.16e. In addition, no samples were presented as a cyclic prefix and no remaining null or pilot subcarriers were constituents for either the guard frequency band or synchronization since they may be independent of the flicker noise effect. For the purposes of calculating bit error rate (BER), this researcher generated the 200 OFDM symbols with four-times over-sampling. This researcher also adopted an additive white gaussian noise (AWGN) channel model for the simulation and assumed perfect channel estimation and synchronization. The overall specifications for the OFDM systems are summarised in Figure 4.3.

4.2.2 Error correction coding

To investigate whether error correction coding can improve flicker noise effect on OFDM systems, this researcher adopted Reed Solomon (RS) convolutional coding in the system. The RS code improves BER performance of the system at a target SNR. Furthermore, variable-rate coding, which can offer the possibility of providing different degrees of protection to the data, is often required in system design [25]. For these

purposes, most OFDM communication systems adopt the RS code for forward error correction coding (FEC) in mandatory [21, 22].

This researcher coded the data field in the OFDM with the convolutional encoder using a coding rate of 1/2, 2/3, or 3/4, which corresponds to the desired data rate in the systems [21,22]. The *m/n* coding rate was defined using the m-bit original information symbol that was transformed into an n-bit encoded symbol, $n \geq m$. In these simulations, this researcher chose the 3/4 coding rate, since the rate is used for high data

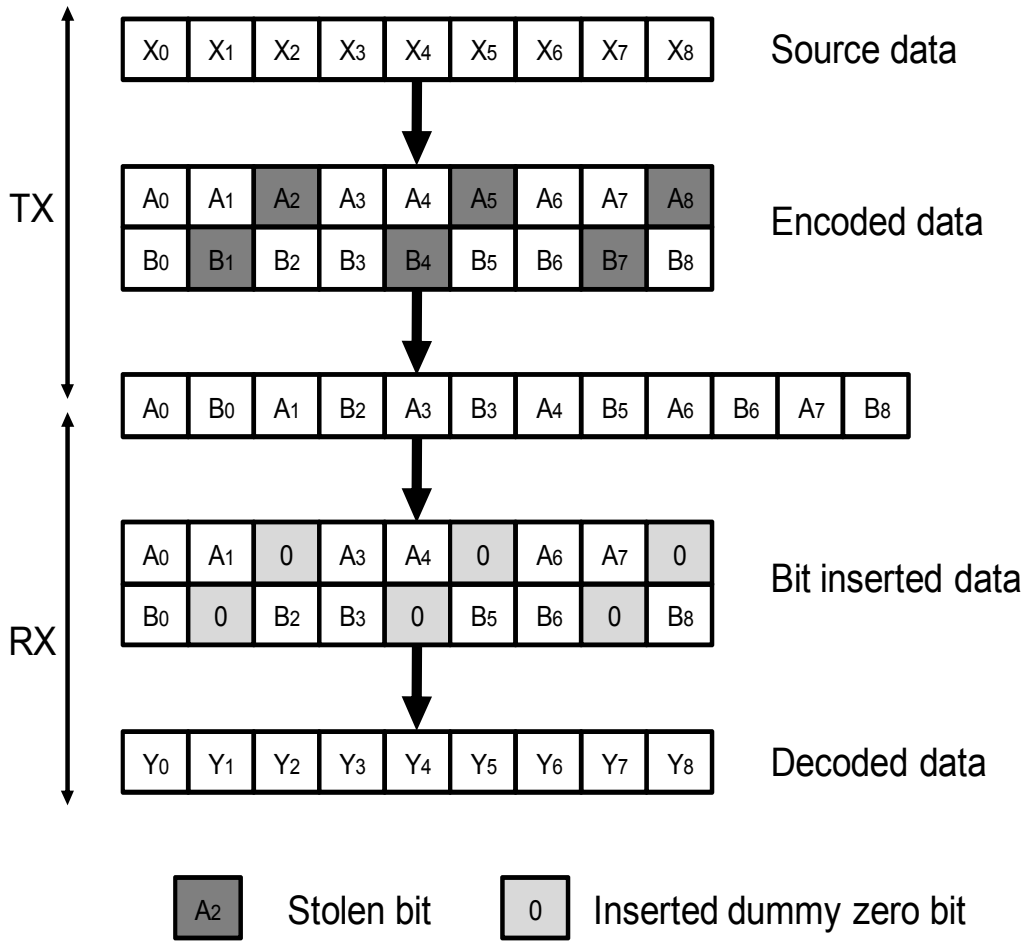


Figure 4.4 : Puncturing process for a 3/4 coding rate.

rate mode in these systems. The convolutional encoder operates 1/2 coding rate and uses the industry-standard generator polynomials, g0=1338 and g1=1718, with 7-bit memory registers. The rate of 3/4 is derived from that of 1/2 by using puncturing function. Puncturing is a procedure for eliminating a number of encoded bits in the transmitter and inserting a dummy zero metric into the convolutional decoder on the receiver in the position of the omitted bits. Thus, this process reduces the number of transmitted bits and increases the coding rate, shown in Figure 4.4. The decoding process was performed by the Viterbi algorithm, which provided maximum likelihood performance and simple implementation.

4.3. Flicker noise models

All of the RF building blocks after DC frequency conversion contribute to the flicker noise. The RF building blocks that are affected by the flicker noise are classified as either switching components, such as mixers, or linear components, such as variable gain amplifiers (VGAs) and filters. In the switching components, the generation of flicker noise is explained by a direct and an indirect mechanism. The direct mechanism is referred to as the generation of flicker noise due to sampled signals in on/off transition time by finite slope of the switching circuit transition. Normally, the differential switching stage turns on/off alternately, and the output current, I, appears alternately as well. However, if the switching operation is not ideal, due to devices or signal mismatches, both switching pairs turn on simultaneously during a transition period. In this event, output current with an amplitude of $2I$ is generated at the switching stage output. This output current samples output noise of the switching stage with a half of LO

period. Thus, in the frequency domain, the sampled noise generates a flicker noise shape around DC and twice the LO frequency. In contrast, the indirect mechanism is defined as the generation of noise according to sampled signals by the charging and discharging of the parasitic capacitance. Even though a sharp signal swing is applied to reduce flicker noise by the direct mechanism, the indirect mechanism flicker noise still exists due to the parasitic capacitance at the common switching node.

On the other hand, there are no universal mechanisms to describe the flicker noise in linear components; however, a charge trapping and releasing model is normally accepted in CMOS technology. The interface between the gate oxide and the silicon substrate in a MOSFET entails this phenomenon. Since the silicon crystal reaches an end at this interface, many dangling bonds appear, giving rise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing flicker noise in the drain current. Unlike thermal noise, the average power of flicker noise cannot be predicted easily. Depending on the cleanness of the oxide-silicon interface, flicker noise may assume considerably different values and as such varies from one CMOS technology to another. The flicker noise is more easily modeled as a voltage source in series with the gate and roughly given by

$$\overline{V_n^2} = \frac{K}{C_{OX}WL} \times \frac{1}{f}, \tag{4.1}$$

where K is a process-dependent constant. The noise spectral density is inversely proportional to the frequency. For example, the trap-and-release phenomenon associated with the dangling bonds occurs at low frequency more often. For this reason, flicker noise is also called *1/f* noise.

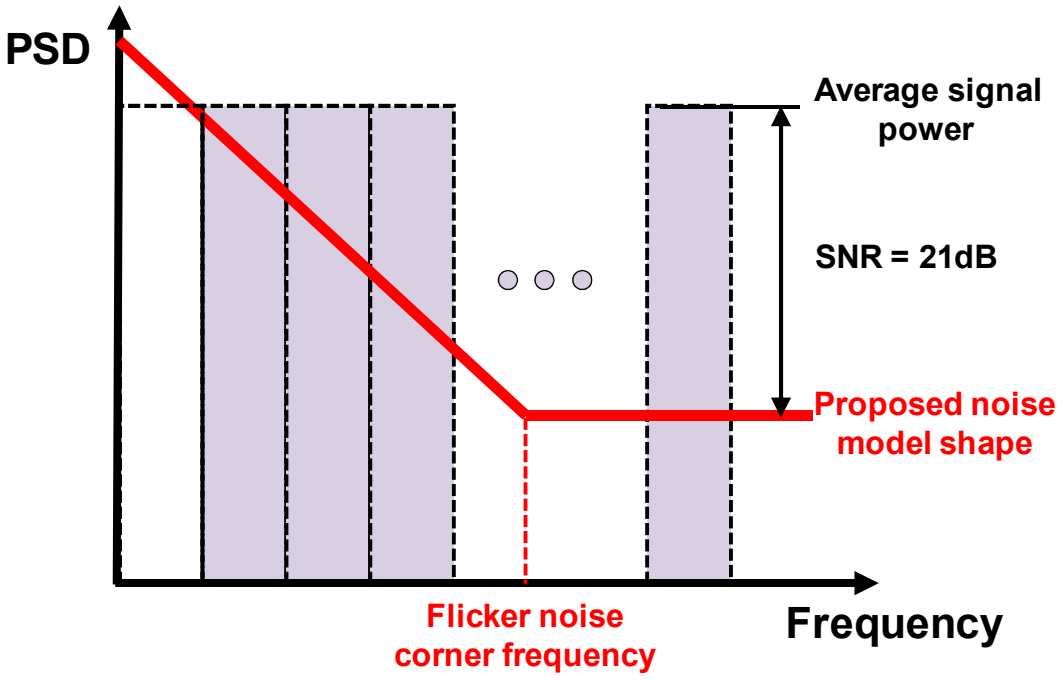


Figure 4.5 : A proposed flicker noise model shape with corner frequencies.

The proposed flicker noise model that includes switching and linear flicker noise is inserted in the RF circuitry. For an approximate prediction of noise power spectral density for flicker noise, a simplified flicker-noise shape model, including a frequency variation, is as follows.

$$P(f) = \frac{K}{f^{\alpha}}, \tag{4.2}$$

where K is the constant for the magnitude of flicker noise and α is its shape factor. This researcher selected an α value of 0.8 by referring to the measured results in the RF components [26]. The flicker noise corner frequency, shown in Figure 4.5, was determined when a required SNR was assumed to be 21dB for 64QAM and 3/4 channel coding in 802.16e [22]. From the SNR value, this researcher can analogize the K value

with (4.2) for the corner frequency. When the flicker-noise shape model is applied to the system simulation, the noise shape should be mixed with random noise for a realistic environment.

$$N_F = \sqrt{P(f)} \times N_R , \tag{4.3}$$

where N_R is random noise with a power of 1. This noise power was generated by a random noise function to have a signal average value of 0 and a signal variance of 1 in MATLAB™. The flicker noise power, N_F, was allocated around the DC frequency, and its even function was mapped around the sampling frequency. Moreover, this researcher also assumed that the AWGN channel corresponds to the SNR.

$$n_{AWGN}(t) = ifft\ (N_R \times \sqrt{\frac{s_{avg}}{2 \times SNR}}) , \tag{4.4}$$

where S_{AVG} is the average signal power of a transmitter. The *ifft* in (4.4) refers to the inverse fast-fourier transform, which converts the time domain signal from the frequency domain signal. In addition, SNR value was multiplied by 2 to create a noise power of 1 in AWGN noise. In the simulation block, the time domain AWGN and the flicker noise were added to transmitted signal *s(t),* forming the received signal *r(t).*

$$r(t) = s(t) + n_F(t) + n_{AWGN}(t) \tag{4.5}$$

4.4. Simulation results

By using the proposed flicker noise model, this researcher investigated the effects of flicker noise on the BER performance of OFDM systems. In addition, this researcher observed how the performance could be enhanced through RS channel coding. As the RS code would improve system reliability and performance in terms of the required BER at a

target SNR, most OFDM communication systems adopt the RS code for forward error correction (FEC) of channel coding in mandatory [21, 22].

Figures 4.6 and 4.7 illustrate the BER curves due to flicker noise when RS convolution coding is absent and when it is present, respectively. For one, this researcher simulated the BER with various corner frequency points without channel coding, shown in Figure 4.6. The corner frequency of flicker noise was chosen as decade values that may be practically implemented in RF components using various technologies. During the simulation, this researcher noticed that BER performance was very sensitive to the corner frequency of flicker noise at a high SNR. Due to increases in the corner frequency, which illustrates larger flicker noise, BER performance degrades and its curves may not reach a zero-error point, even in a high SNR region.

In Figure 4.7, the BER performance of RS convolution codes with different flicker noise corner frequencies for the OFDM was presented. This researcher assumed the 3/4 rate RS code since 64 QAM is used for the high data rate mode in various systems [21, 22]. The results indicate that a coded signal with flicker noise performs slightly better than an un-coded signal at high SNR values.

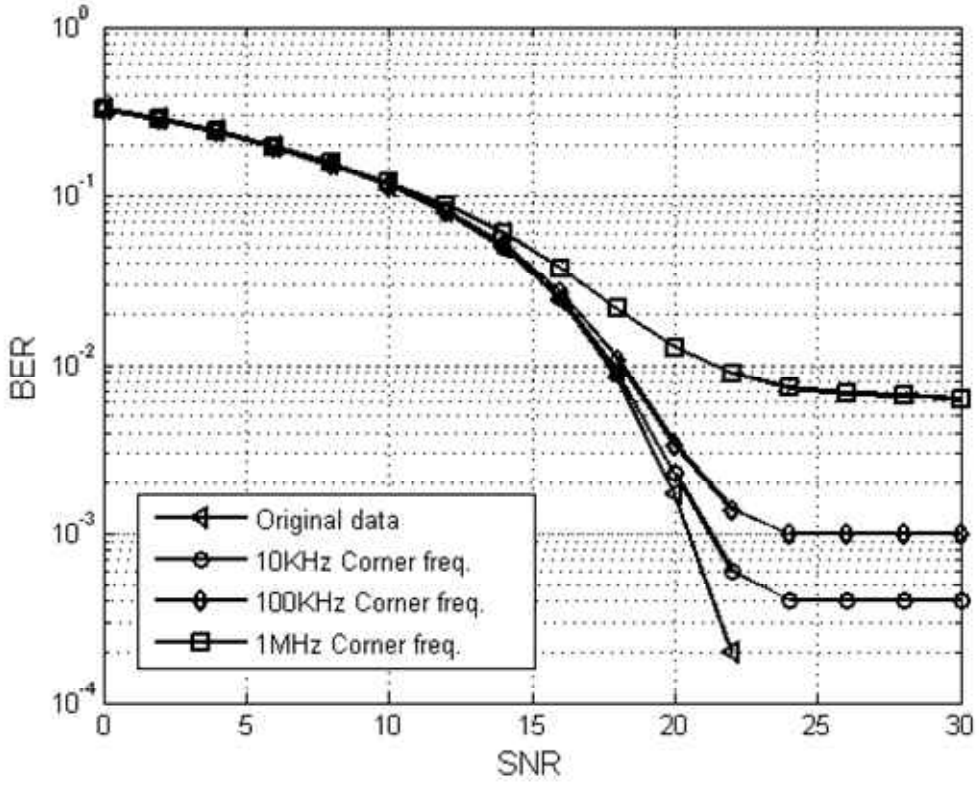


Figure 4.6 : BER performance for different corner frequencies with raw data.

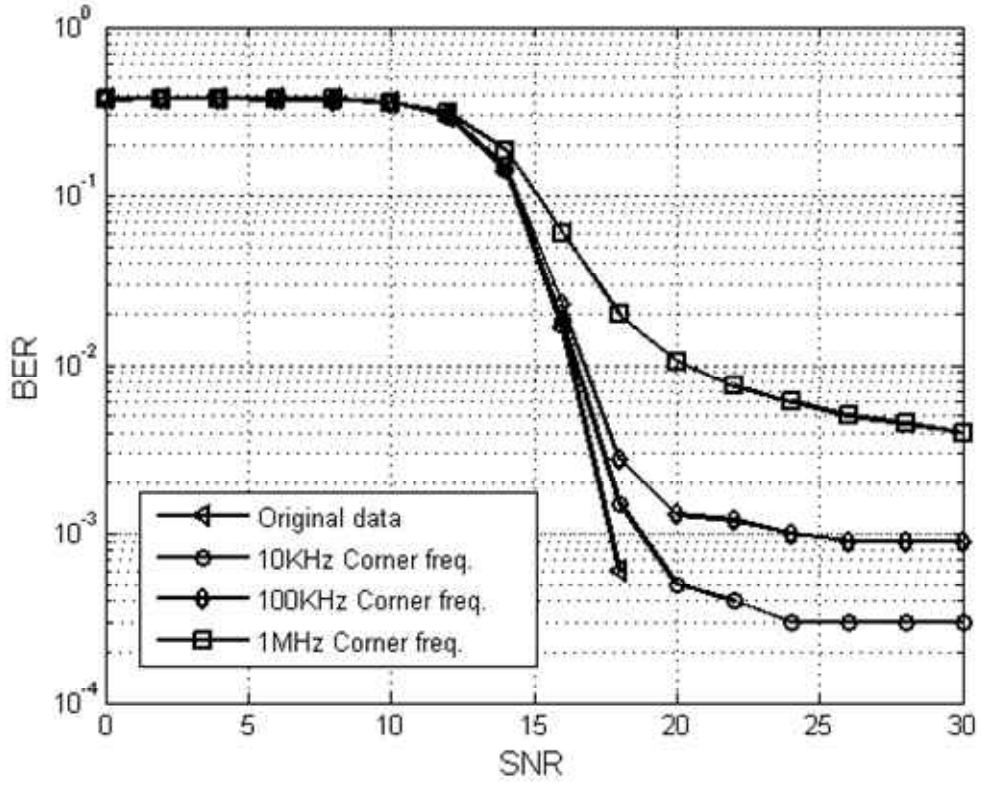


Figure 4.7 : BER performance for different corner frequencies with RS convolution- coded data.

4.5. Summary

This researcher proposed a flicker noise model for the simulation of OFDM systems and measured its effect on the system. This investigation found that flicker noise may degrade BER performance in high SNR conditions. Even if this researcher increased the required SNR for OFDM systems, performance degradation, due to flicker noise, would still occur. As the RS decoder was not able to detect and correct all errors caused by flicker noise, channel coding, using RS decoders, may not be capable of reversing degradation.

V. LOW FLICKER NOISE CMOS MIXER DESIGN

5.1. Introduction

From the results of the previous section, it is obvious that the flicker noise degrades system performance and the system performance cannot be improved by modem techniques, such as error-correction coding. For solving the flicker noise issue in RF domain, a low flicker noise CMOS mixer is proposed in this section. From the section 2, it is mentioned that flicker noise is dominantly generated from the mixer when the direct conversion architecture is applied. In addition, CMOS technology is more vulnerable to flicker noise because it is the surface oriented device as mentioned the section. Thus, the implementation of a low flicker noise CMOS mixer is the efficient and sole way for low flicker noise RF receiver.

Section 5.2 shows the mixer topologies including active and passive mixers. In addition, Gilbert-cell active type mixer is investigated. 5.3 presents the conventional approaches for low flicker noise CMOS mixer. This section focuses on flicker noise reduction technique in the active mixer. In section 5.4, flicker noise mechanisms of the mixers are discussed. In addition, it presents that local oscillator (LO) phase mismatches are the dominant cause of flicker noise in the mixer. Section 5.5 shows the concept of the proposed low flicker noise mixer, and Section 5.6 illustrates the experimental results of the mixer.

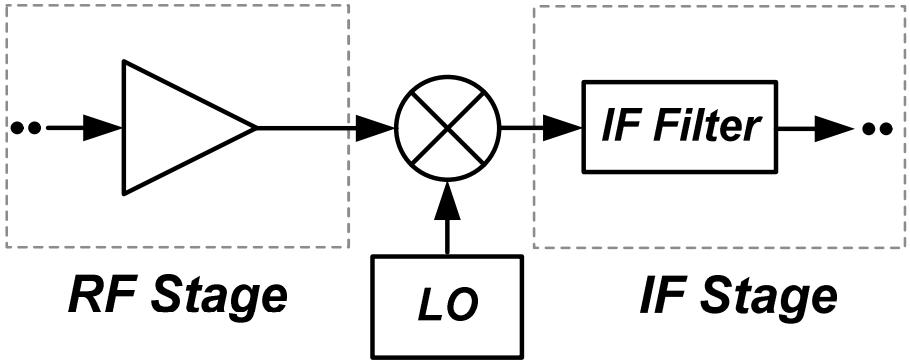


Figure 5.1 : Block diagram of a mixer in RF architecture.

5.2. Mixer topologies

5.2.1 Roles of mixer in RF architecture

The down-conversion mixer translates an incoming RF signal to a low frequency known as the intermediate frequency (IF), shown in Figure 5.1. In the direct conversion architecture, the frequency of the IF stage is started from DC. The IF stage facilitates to obtain the requisite high gain and high stability in RF receivers because it provides high isolation between the RF stage and the IF stage by using different frequencies. Through the mixer, the selection of channel frequency is accomplished by varying the frequency of a local oscillator (LO), rather than by varying the center frequency of the IF filter. Thus, the channel frequency is effectively selected by a single LC combination of the local oscillator. In addition, the low IF frequency enhances selectivity of RF parts in the system because the IF stages uses fixed-frequency filters, which are much easier to implement for having high rejection performance of interferes rather than variable frequency filter. Moreover, the overall gain of the system is distributed to various frequency bands, and then the required total receiver gain is achieved without the much

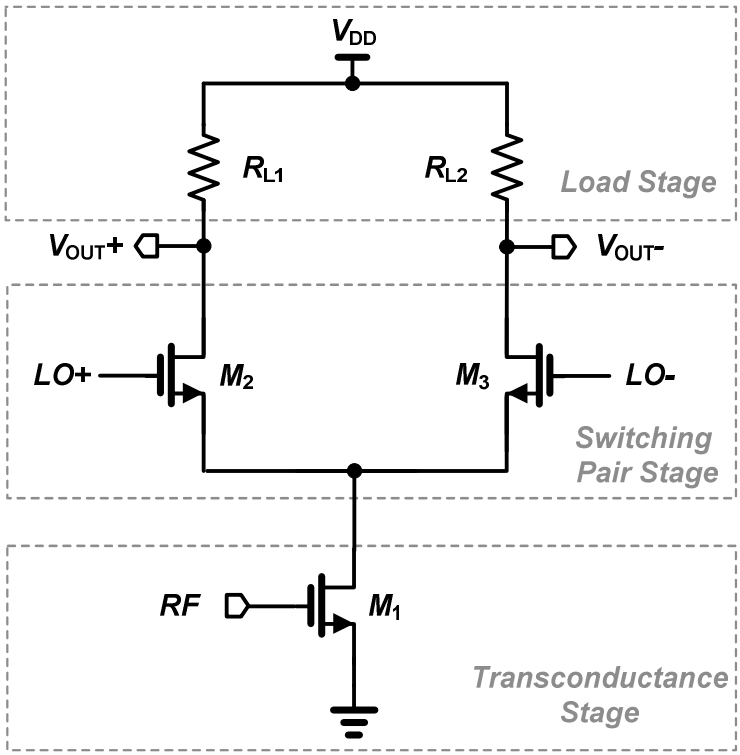


Figure 5.2 : Active mixers.

consideration of the stability in circuits. In addition, the requirement of linearity in the IF stage can be mitigate since inter-channel interferers are easily eliminated by fixed-frequency IF filters.

5.2.2 Active and passive mixers

Mixer topologies are normally classified as active mixers and passive mixers. The active mixer generally provides high voltage gain because it has bias current in the switching pair stage, shown in Figure 5.2. The RF incoming signal varies the drain current of M_1, and the switching pair stage consisting M_2 and M_3 is driven by LO signal.

The drain current of M_1 is multiplied by a square wave version of the LO signal and it is routed to R_{L1} and R_{L2} in the load stage, alternatively. The gate biasing in saturation region with a proper choice of size of M_2 and M_3 can provide significant voltage gain of the active mixer. With a help of voltage gain, the active mixers offers lower noise than passive type mixers.

On the other hand, passive mixers, which are not provide any gain, have some attractive properties, such as the potential for low power consumption because it has no bias current in switching pair stage. In addition, the passive mixers provide high linearity since it has small output voltage swing. The small output swing is originated from no voltage gain in passive mixers. Moreover, the flicker noise of passive mixers is low with a help of no bias current in the switching pair. However, it requires the large voltage swing of local oscillator signal for acting as ideal switches in the passive type. In addition, the passive mixers do not provide conversion gain that can alleviate the gain and noise requirements of the proceeding building blocks. Even though passive mixers are generally used in RF systems for modern wireless communications terminals, the active type mixer is more efficient to apply low noise RF systems. Thus, in this research, we focus on active type mixer, which has high gain and low thermal noise, in order to implement low noise RF systems.

5.2.3 Gilber-cell active mixers

For designing active mixers, a double-balanced Gilbert-cell topology has been widely employed because of its high port-to-port isolation. Figure 5.3 represents schematic

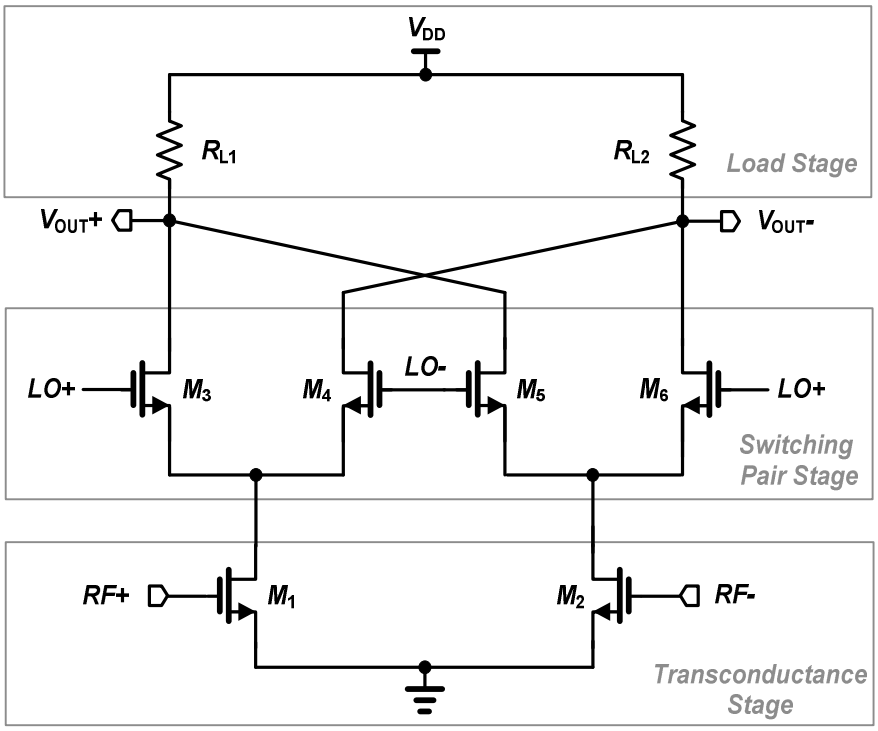


Figure 5.3 : Gilbert-cell active mixers.

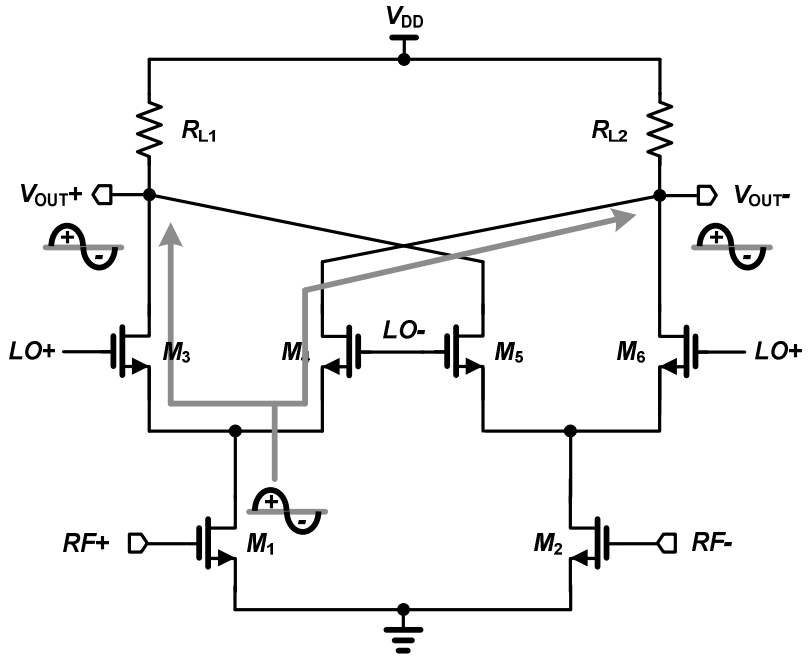
diagram of conventional Gilbert-cell active mixer configuration. The differential pair M_1 and M_2 of the circuit is referred to as a transconductance stage converting a RF voltage signal into a current. The differential pairs M_3 to M_6 are defined as switching pair stages acting as switching pairs driven by LO signals. The load stages consist of R_{L1} and R_{L2}, which are used as load resistance for loading very low IF frequency in the direct conversion architecture.

The isolation between each port is critical in RF systems. The LO-RF feedthrough generates LO leakage and a finite amount of LO leakage appears at the input of LNA. The following mixer is mixed with the amplified LO leakage according to the LNA and the LO signal itself in direct conversion architecture. This phenomenon is called as self-mixing and it produces DC offset, which can corrupt the signal and saturate the following stages. The LO-IF feedthrough and RF-IF feedthrough are also important because the LO

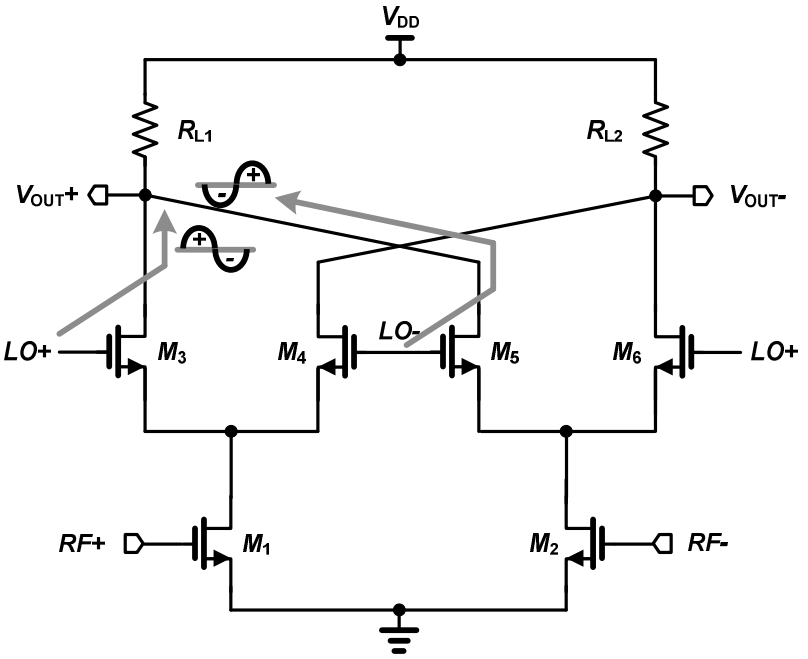
and RF leakage in IF output can desensitize the following stage. Even though the required isolation levels depend on the application the mixer is used, the isolation levels in direct conversion need to be as high as possible.

In the double-balanced Gilbert-cell topology, the high isolation between LO-to-RF ports is achieved by dual gate configuration. The dual gate configuration can be defined as the structure that LO signal and RF signal are injected from different gates of transistors in the mixer. The separate ports between LO and RF offers high isolation because the leakage from LO to RF is only occurred through parasitic capacitance of the transistors.

The RF-IF feedthrough and the LO-IF feedthrough in the Gilbert-cell mixer are conceptually explained in Figure 5.4. The RF-IF feedthough in the Gilbert-cell is canceled out according to a double-balanced structure. The RF signal converted to current from M_1 flows to M_3 and M_4 simultaneously at the switching pair transition time when both M_3 and M_4 are turns on without the frequency conversion. These two same phase RF signals in output ports can be eliminated by the balanced configuration. The rejection of the RF-IF feedthough from the signal of M_2 can be explained as the same mechanism as well. Thus, in the IF output port, the RF-IF feedthrough is not observed when no mismatches in balance structure are supposed. The Gilbert-cell mixer also rejects LO-IF feedthrough. From Figure 5.4, the positive LO leakage arising from parasitic capacitance of M_3 and the negative LO leakage arising from that of M_4 are canceled out in the positive IF output port. Thus, LO-IF feedthrough is eliminated at the output when LO signal mismatches are ignored. The LO leakages from M_5 and M_6 can be described as the same explanation.



(a)



(b)

Figure 5.4 : (a) RF-to-IF port isolation in Gilbert-cell active mixers (b) LO-to-IF port isolation in Gilbert-cell active mixers.

From these port-to-port isolation advantages, this research chooses the Gilbert-cell type active mixer as a basic configuration. However, the Gilbert-cell active mixer still has much more flicker noise than the passive type mixer since it operates typically in high bias current, which can increase the flicker noise of devices. Moreover, as the conversion gain of the Gilbert-cell mixer is proportional to a load resistance, a large resistance of the load is required to obtain high conversion gain. The large load resistance results in low voltage headroom, which degrades the linearity of the mixer [27]. Thus, the conventional Gilbert-cell active mixer exhibits high flicker noise and restricted conversion gain.

5.3. Flicker noise mechanisms in Gilbert-cell active mixers

5.3.1 Flicker noise contributions

The Gilbert cell mixers comprise the transconductance stages, switching pair stage, and load stage as described previous sections. In direct conversion receivers, the load stages are generally implemented by resistors, R_{L1} and R_{L2}, shown in Figure 5.3. As a LC tank, which is another candidate for load stage, is difficult to apply in the direct conversion due to its huge size for DC frequency, resistors are generally used for the load stage in the integrated circuit at the expense of voltage headroom. For the resistor, a polysilicon type resistor is normally utilized because it offers precise value and lower parasitic capacitances. Moreover, the polysilicon resistor is free of flicker noise [28]. Thus, we don't need to consider flicker noise contribution of the polysilicon resistor load stage.

For the transconductance stage, the flicker noise of the stage is up-converted to LO frequency and to its odd harmonics. Thus, in the output DC frequency, the flicker noise from the transconductance stage cannot be observed if no mismatch of switching pair stage is supposed [28]. Thus, the flicker noise of mixer is mostly generated from switching pair stage

5.3.2 Flicker noise in the switching pair stage

In the Gilbert-cell mixer shown in Figulare 5.3, switching pair stage transistors should turn on or off alternatively. When M_3 and M_6 of the switching pair are turned on, M_4 and M_5 should turn off, and vice versa. However, in the transition time of turning on or off, the operation of the switching pair can be classified as either in the ON or OFF overlap mode according to the gate bias of the switching pair stage. The ON/OFF overlap modes are defined as the transition time when the switching pair stage is switched at both ON or both OFF states, respectively. Figure 5.6 represents ON and OFF overlap mode operations with an in-phase LO signal, $V_{LO}+$, and an out-of-phase LO signal, $V_{LO}-$, where both are operated at LO frequency with no phase mismatch. V_G and V_S represent the gate and the source DC bias voltage of the switching pair transistor from M_3 to M_6, respectively. The ON overlap mode occurs at $V_G > V_S + V_{TH}$, where V_{TH} is the threshold voltage of the device, while the OFF overlap mode takes place at $V_G < V_S + V_{TH}$.

When the ON overlap mode is supposed, the flicker noise of the switching pair stage in the Gilbert-cell mixer is normally explained by the direct and the indirect mechanism [28]. The direct mechanism is the flicker noise generation due to sampled signals in on/off transition time by the finite slope of the switching circuit transition. In contrast, the

indirect mechanism is defined as the noise generation due to sampled signals by charging and discharging of the parasitic capacitances at the node between the transconductance and switching pair stages. According to the direct mechanism, the leaking signals of the switching pairs to the output during the ON overlap mode produce flicker noise. In this ON overlap switching event, an output current with $2I$ amplitude is generated at the mixer output, shown in Figure 5.6. In addition, flicker noise at the gate of switching pairs presents at the mixer output without frequency conversion [28]. In this case, the output current with an amplitude of $2I$ samples the output flicker noise, V_n, with a LO period over 2 and generates flicker noise shape at DC and at even harmonics of LO frequency in the frequency domain. This flicker noise has higher spectral density than that of the gate in the switching pairs because the spectral density of the flicker noise is multiplied by $4I/ST$, where S is the slope of the LO signal and T is the period of LO [28]. This flicker noise generation is referred to as the direct mechanism and it is proportional to output current I.

Even when a sharp LO signal swing is applied to reduce flicker noise by the direct mechanism, the indirect mechanism flicker noise still exists due to parasitic capacitances at the node between the transconductance stage and the switching pair stage [28].

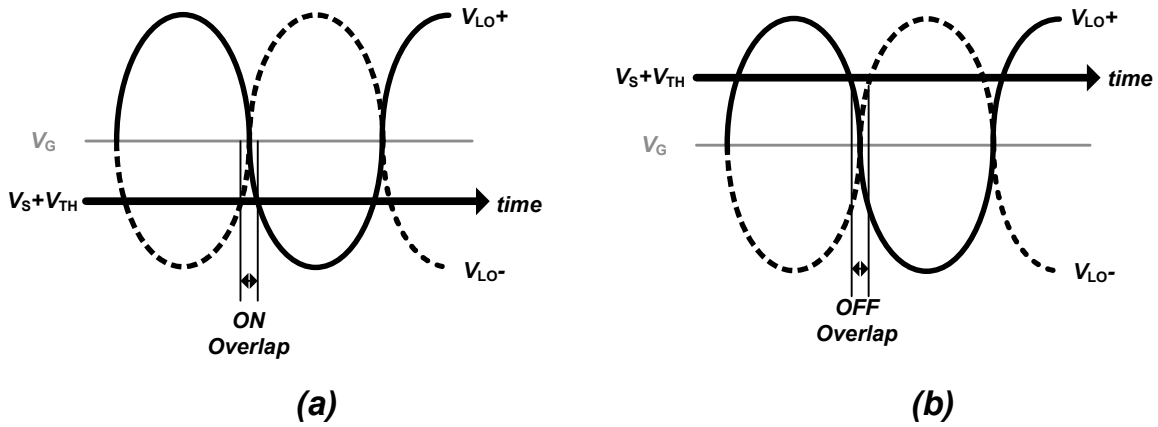


Figure 5.5 : Operation of switching pairs. (a) ON overlap mode without phase error. (b) OFF overlap mode without phase error.

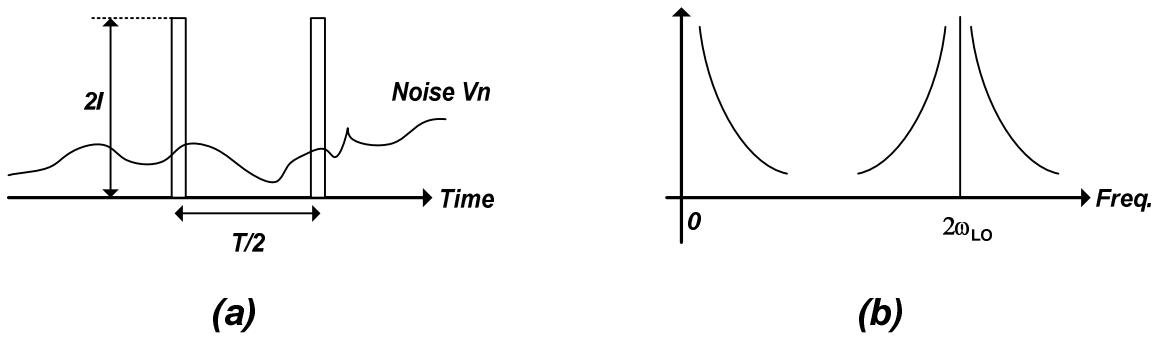


Figure 5.6 : Flicker noise generation of ON overlap mode (a) Time domain analysis. (b) Frequency domain analysis.

5.4. Conventional flicker noise reduction Techniques

5.4.1 ON overlap mode

To reduce the ON overlap mode flicker noise and to overcome gain limitations of the conventional Gilbert-cell active mixer, a current bleeding technique has been reported [29]. Figure 5.7 shows the simplified half circuit schematic diagram of a Gilbert-cell mixer with the current bleeding technique. By adding current-bleeding paths between the transconductance and the switching pair stages, the bias current in the switching pair stage is reduced, while that of the transconductance stage is maintained. The reduced bias

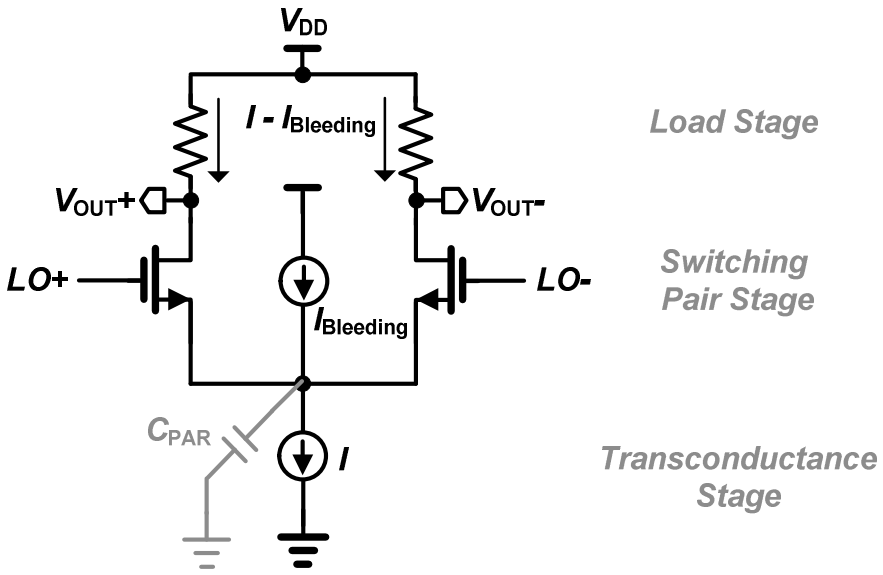


Figure 5.7 : Schematic of the conventional Gilbert-cell mixer with current bleeding.

current of the switching pair stage improves flicker noise performance due to the low height of the noise pulse [30]. The low height of the noise pulse, described as 2*I* in Figure 5.6, reduces the flicker noise from the direct mechanism because it reduces noise power in the frequency domain. In addition, as a part of the bias current in the transconductance stage is steered from the current bleeding circuit, R_{L1} and R_{L2} can be increased while maintaining the drain-to-source bias voltages of the transconductance stage and the switching pair stage. Thus, through the current-bleeding technique, the large load resistance of the load stages provides higher conversion gain than conventional Gilbert-cell configurations [31].

Although the current-bleeding technique can enhance flicker noise and conversion gain, the additional noise source due to the presence of the bleeding circuit increases the thermal noise figure [32]. In addition, the bleeding circuit itself offers more parasitic capacitance, C_{PAR}, generating flicker noise from the indirect mechanism [32]. As a result, the current-bleeding technique has the limitation of enhancing flicker noise due to C_{PAR}.

Furthermore, reduced bias current in the LO stages allows the RF signal to be shunted by parasitic capacitances since the impedance, as seen from the source of LO stages, $1/g_m$, is increased [30]. Due to parasitic capacitances, the current-bleeding technique degrades the bandwidth and the linearity of the mixer as well.

To reduce or tune out the parasitic capacitances, which degrade bandwidth, linearity, and flicker noise, series and parallel connections of inductor techniques in the current-bleeding mixer have been reported [33, 34]. In [33], a parallel inductor in the bleeding circuit is used to tune out the parasitic capacitor at twice the resonant frequency, $2f_0$, to enhance linearity and flicker noise. In contrast, series connected inductors in the bleeding circuit are employed to resonate out the parasitic capacitor at f_0 to improve flicker noise [34]. However, in both techniques, as the required inductance for tuning out parasitic capacitance is relatively large, these topologies occupy a large die area. In addition, the large inductance, which results in a low self-resonant frequency, limits the frequency range of applications. Alternatively, a dynamic current-bleeding technique has been reported to improve flicker noise performance [30]. This technique injects a current that is equal to the bias current in the RF stage when an LO switching transition occurs. However, the technique is effective only to reduce flicker noise when an ON overlap mode is supposed.

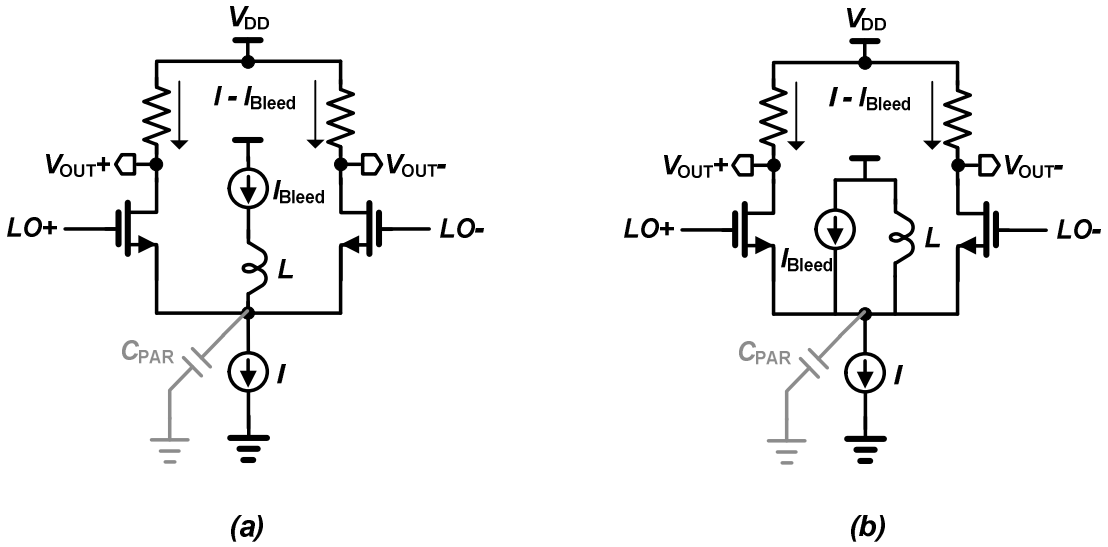


Figure 5.8 : Simplified schematic diagram of the conventional Gilbert-cell mixers. (a) series inductor connection. (b) parallel inductor connection.

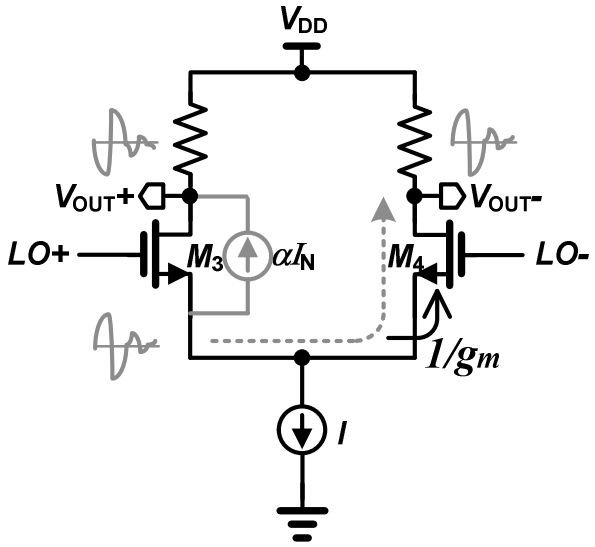


Figure 5.9 : Simplified schematic diagram for noise analysis in ON overlap mode.

Furthermore, the ON overlap mode increases the noise figure of the mixer. In Figure 5.9, the thermal channel noise of M_3 experiences low input impedance, $1/g_{m4}$, of M_4 during the ON overlap mode. Due to the low input impedance, a large amount of the thermal channel noise in the switching pairs flows to the differential output as out-of-phase. Thus, the thermal channel noise of the switching pairs contributes to the noise

figure in the ON overlap mode. Moreover, the ON overlap mode degrades the linearity of the mixer. During the ON overlap time, the gate to source capacitances, C_{gs}, of the switching pairs act as a nonlinear shunt distorting the output current of the mixer [29]. However, conventional flicker noise reduction techniques cannot enhance the degradation of the noise figure and are effective only at reduceing flicker noise in the ON overlap mode.

5.4.2 OFF overlap mode

OFF overlap mode biasing is proposed to eliminate the direct mechanism of the flicker noise by preventing both LO switches from turning on at the same time [23]. In addition, the discharge process due to the linear region of the transconductance stage in the OFF overlap mode reduces the flicker noise from the indirect mechanism [35]. In the OFF overlap mode, both switching pairs turn off simultaneously at a transition time by biasing the gate voltage, which is $V_G < V_S + V_{TH}$. In this case, the OFF overlap mode can reduce flicker noise because sampled output noise current cannot be generated, as shown in Figure 5.10. In addition, the OFF overlap mode can reduce thermal noise because no channel noise is generated from the switching pair stage in the OFF overlap time.

Even though the OFF overlap mode can reduce flicker noise and thermal noise of the mixer, it suffers from lower conversion gain and lower IIP3 than does the ON overlap mode, as shown from experimental results in [23]. As the RF signal is not converted to an IF signal at the OFF overlap mode transition time, a portion of the output signal is lost at this moment. This lost output signal results in degradation of conversion gain. In addition, IF signal discontinuity according to OFF overlap time results in degradation of linearity.

5.5. Flicker noise mechanisms from LO phase mismatches

From these characteristics, operation either in the ON or OFF overlap mode can be chosen by a designer considering the prior performance of the mixer because each overlap mode has its advantages. Generally, the performances of mixer are optimum when the $V_G = V_S + V_{TH}$. However, LO phase mismatches between $V_{LO}+$ and $V_{LO}-$ can generate flicker noise as well. The LO phase mismatch is normally 5 degrees to 10 degrees in the RF systems of wireless mobile terminals. The LO phase mismatch is generated from single- to-differential conversion building blocks, such as an LO balun and a frequency divider, and length mismatching of differential lines. The LO phase mismatches make the mixer operate in the ON and OFF overlap mode alternatively, as shown Figure 5.11.

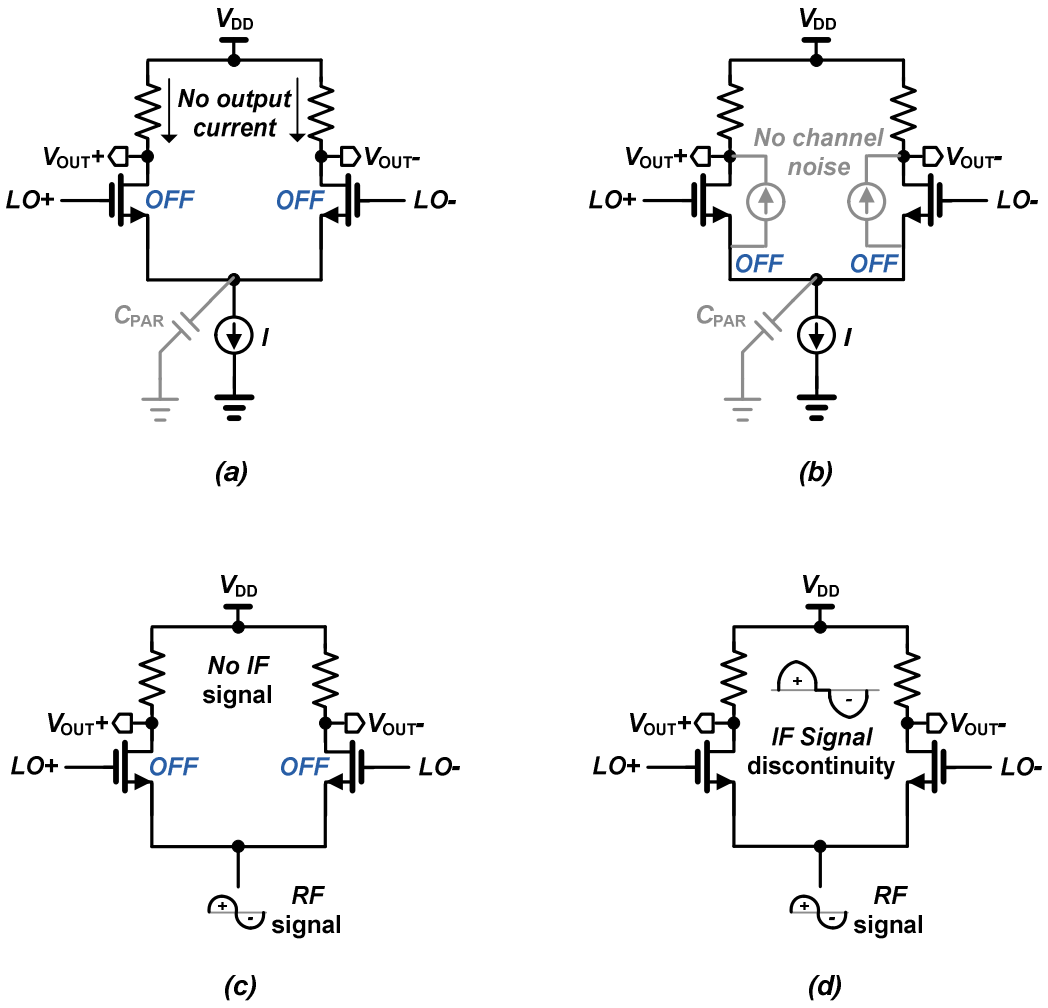


Figure 5.10 : OFF overlap mode operations. (a) Flicker noise reduction. (b) Thermal noise reduction. (c) Gain degradation. (d) linearity degradation.

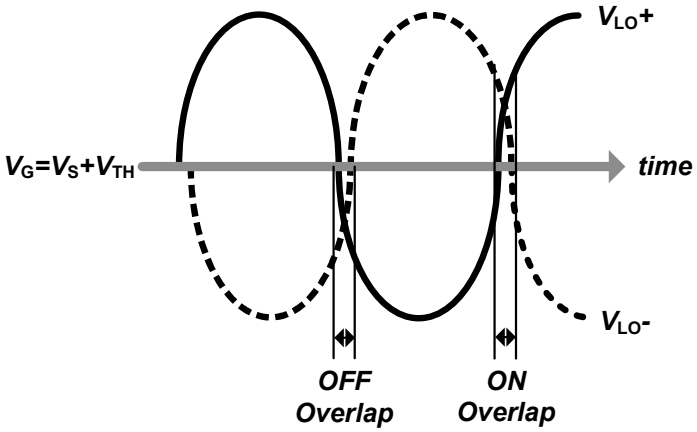


Figure 5.11 : Operation of switching pairs when LO phase mismatches exist.

The effect of LO phase mismatches on flicker noise of the mixer can be explained as follows. During the ON overlap time, output noise pulse trains are generated with a frequency of LO. By the direct mechanism, the average value of the output noise current over one period is [28]

$$i_{0,n} = \frac{1}{T} \times 2I \times \Delta t = \frac{2I \times V_n}{S \times T}, \tag{5.1}$$

where T is the LO period, and I is the DC current of the RF stage. In addition, Δt is the ON overlap time, and V_n is the low frequency noise at the gate of switch. This indicates that V_n directly appears at the output of the mixer without frequency conversion during the ON overlap time. From the frequency domain viewpoint, the output noise current is easily transformed from (5.1) as

$$i_{0,n}(f) = \frac{2I}{S \times T} V_n(f), \tag{5.2}$$

where the $V_n(f)$ has the *1/f* noise spectrum. The images of the output noise spectrum exist at multiples of LO frequency and the image near the DC frequency appears as flicker noise. By the indirect mechanism, the output noise current also appears at the LO frequency in the ON overlap time due to parasitic capacitances between the RF and the LO stage. The output noise current is given as [28]

$$i_{0,n} = \frac{1}{T} \times C_P \times V_n \ , \tag{5.3}$$

where C_P is the parasitic capacitance at the node. Therefore, the flicker noise is generated both by the direct and the indirect mechanism in the ON overlap time according to the LO phase mismatch. In addition, during this time, the noise figure is degraded as explained earlier. In the OFF overlap time according to the LO phase mismatch, the only

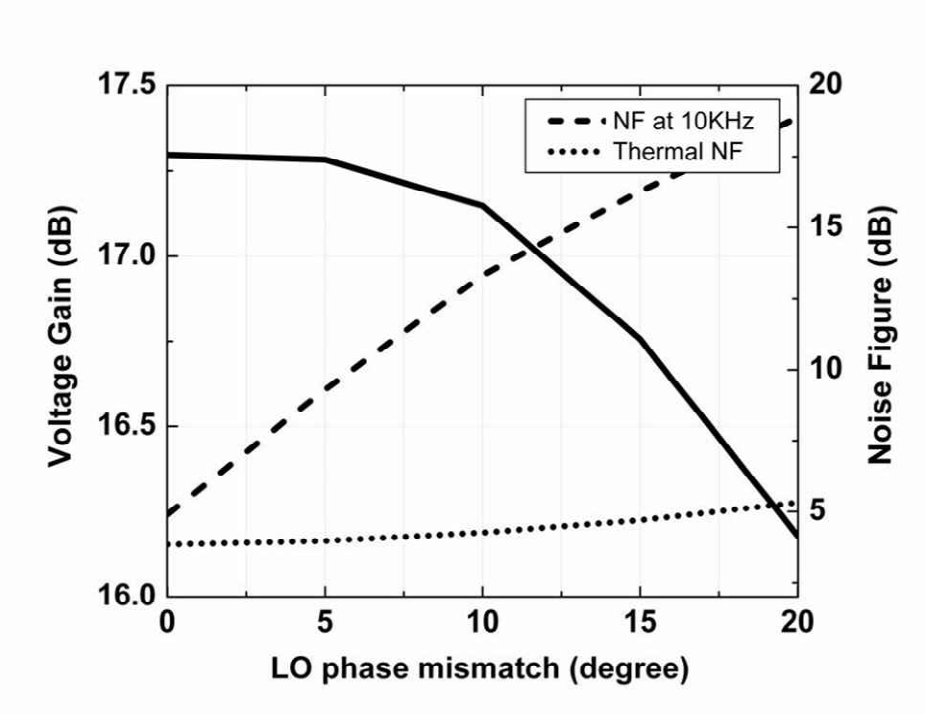


Figure 5.12 : Gain, Noise figure, and flicker noise of Gilbert-cell current bleeding mixer with LO phase mismatch.

benefit of the OFF overlap mode, which is low flicker noise, cannot be applied due to flicker noise generation of the ON overlap time. Furthermore, the OFF overlap time contributes to low conversion gain due to losses of IF signals.

To verify this analysis, the performance of the current bleeding Gilbert-cell mixer with the LO phase mismatches is simulated in Figure 5.12. For the simulation, various phase mismatches are generated from the LO, and the bleeding current of the mixer is fixed to be half of the bias current in the RF stage.

From the simulation results, as expected, the LO phase mismatch degrades conversion gain, noise figure, as well as flicker noise. The more the phase mismatch is generated, the more the performance is degraded. Even though gain and noise figure performances are slightly degraded, the flicker noise is greatly degraded as phase mismatching increases.

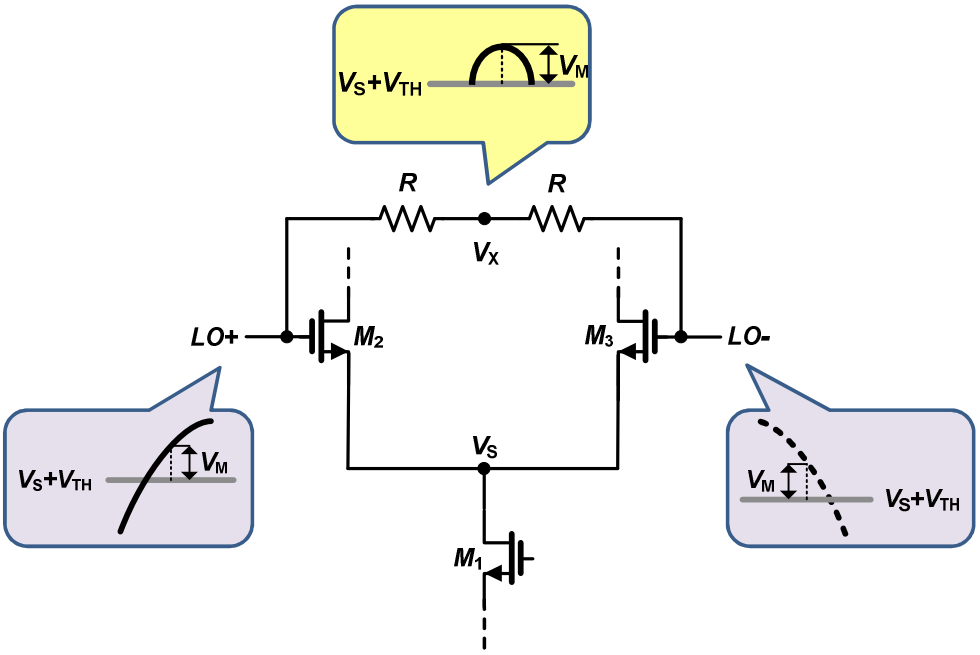
Thus, the LO phase mismatch needs to be compensated to prevent performance degradation of the mixer.

5.6. Concept of the proposed mixer

To alleviate the LO phase mismatch effect on the current bleeding mixer, a detection circuit for the LO phase mismatch should be considered first. In this research, two common mode resistors, connecting to the LO ports in parallel, are proposed for the LO phase detector, as shown Figure 5.13. At the node for common mode voltage, V_X, the average value of $V_{LO}+$ and $V_{LO}-$ is generated. In ON overlap time, if $V_{LO}+$ and $V_{LO}-$ have a lager an amount of V_M than $V_S + V_{TH}$, V_X produces $V_M + V_S + V_{TH}$ at this moment. On the other hand, for the OFF overlap mode, when $V_{LO}+$ and $V_{LO}-$ have a smaller amount of V_M than $V_S + V_{TH}$, V_X produces $-V_M + V_S + V_{TH}$. If the gain and phase between the $V_{LO}+$ and $V_{LO}-$ are perfectly matched, no AC signal is produced at the node V_X . Thus, the parallel-connected resistors in the LO ports can play a role as the LO phase mismatch detector indicating the amount of ON and OFF overlap signal with a simple configuration.

The compensation process for the detected LO phase mismatch is proposed by controlling the source voltage in the LO stage, V_S, as shown Figure 5.14. In the conventional current bleeding circuit, V_S is set to the value maintaining the saturation region of M_1. As mentioned Figure 5.13, the detection circuit of the LO phase mismatch produces larger or smaller AC voltage than V_S+V_{TH} depending on the overlap mode. The compensation processes of the LO phase mismatch can be accomplished by control of V_S. In Figure 5.15, the increased V_S value provides the compensation of the ON overlap time, whereas the decreased V_S value presents that of the OFF overlap time.

For the control of the V_S value, the trans-conductance amplifier is added between the V_X and the V_S node as shown in Figure 5.14. The amplifier senses the output voltage of the detector and translates it into a current, I_S. To load the signal of the detector and to prevent an injection from the RF signal from M_1, the input and the output impedance of the trans-conductance amplifier needs to be high. The output current from the amplifier converts to voltage with an output impedance of M_1. Therefore, the value of V_S changes in proportion to V_X. At the ON overlap time, V_X, which is greater than $V_S + V_{TH}$, increases V_S due to the proposed configuration. On the other hand, V_X, which is smaller than $V_S + V_{TH}$, decreases V_S in the OFF overlap time. Thus, the difference of V_X and $V_S + V_{TH}$ can be greatly reduced in both ON and OFF overlap time. Through this detection and compensation mechanism, the LO phase mismatch now longer contributes to ON/OFF overlap time. Moreover, an inductive load inserted between the trans-conductance amplifier and M_1 can enhance the performance of the operation. The parasitic capacitance at the node V_S prevents the loading from I_S. As the inductive load can partially cancel out the parasitic capacitance, the I_S can be loaded more effectively. From these processes, the ON and OFF overlap time period due to LO phase mismatch is successfully compensated in the proposed mixer topology.



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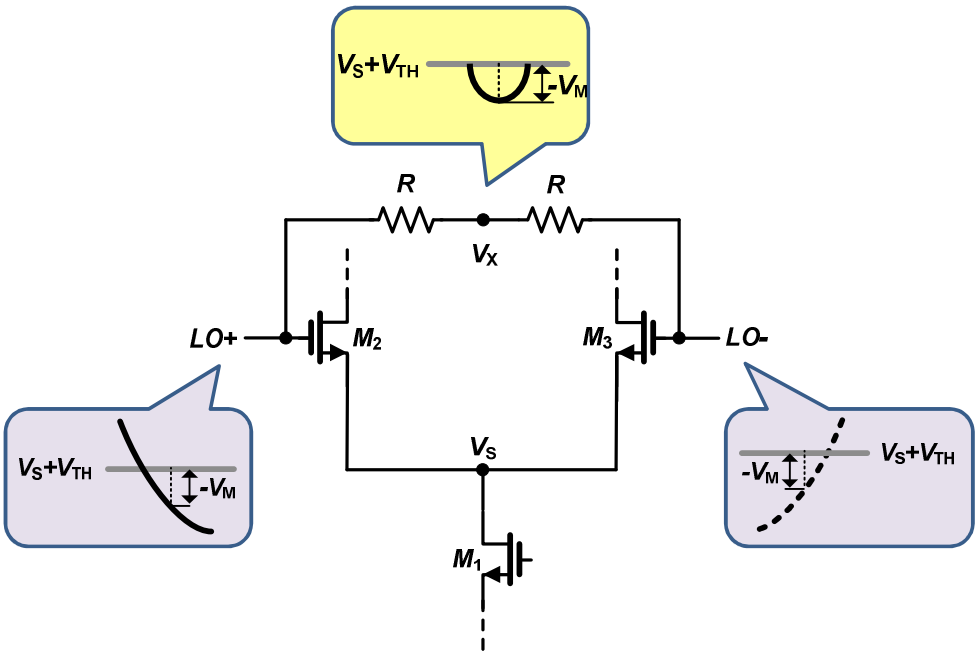


(b)

Figure 5.13 : Schematic of LO phase detector and its operations. (a) ON overlap mode operation. (b) OFF overlap mode operation.

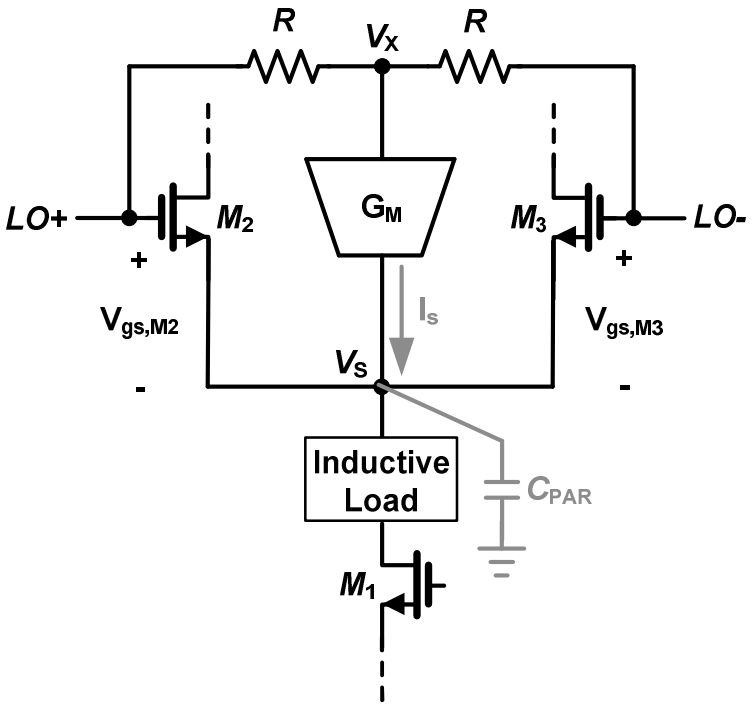
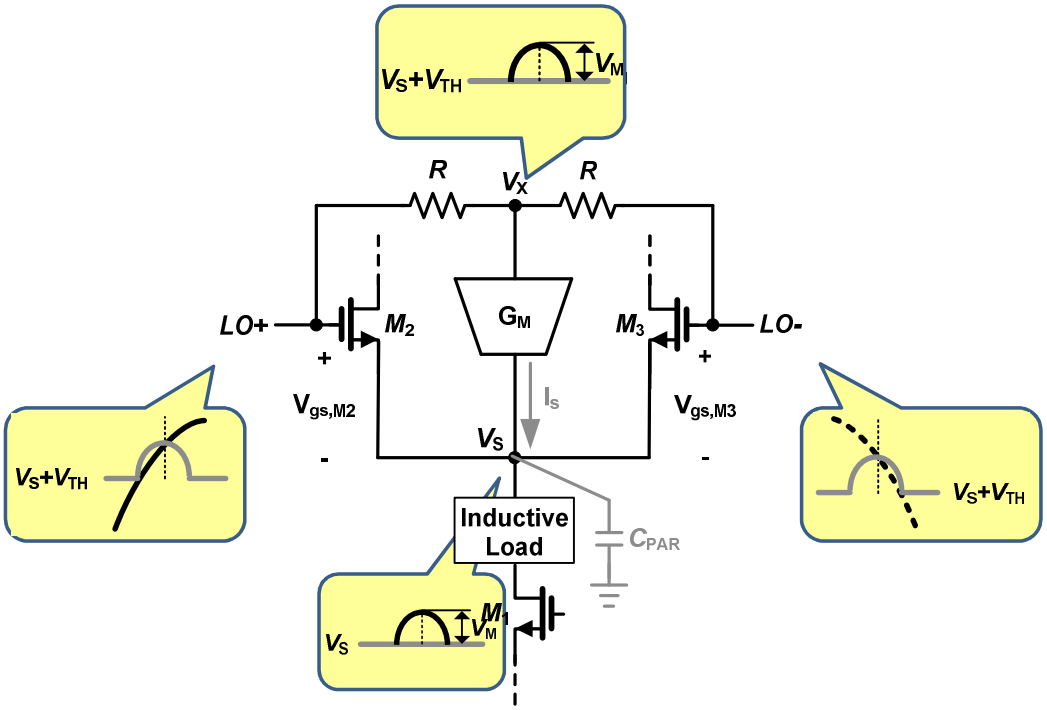


Figure 5.14 : Conceptual diagram of the proposed mixer.

In order to validate this concept, the proposed conceptual idea is fully-implemented in the Gilbert-cell configuration with the current bleeding technique, as shown in the Figure 5.16. M_1 and M_2 are used as the RF stages. In the RF stages, a source degeneration technique is employed to improve input matching and linearity. The degeneration technique is implemented by a bondwire inductor, which has a high Q-factor for low noise. In addition, capacitors, C_{C1} and C_{C2}, between gates and sources of M_1 and M_2 are also added to boost linearity. This is because the value of the degenerated inductor can be increased as the C_{C1} and C_{C2} values are increased while maintaining input matching. The mixer is loaded with poly silicon resistors, R_{L1} and $R_{L2,}$ in order to free of flicker noise [30].



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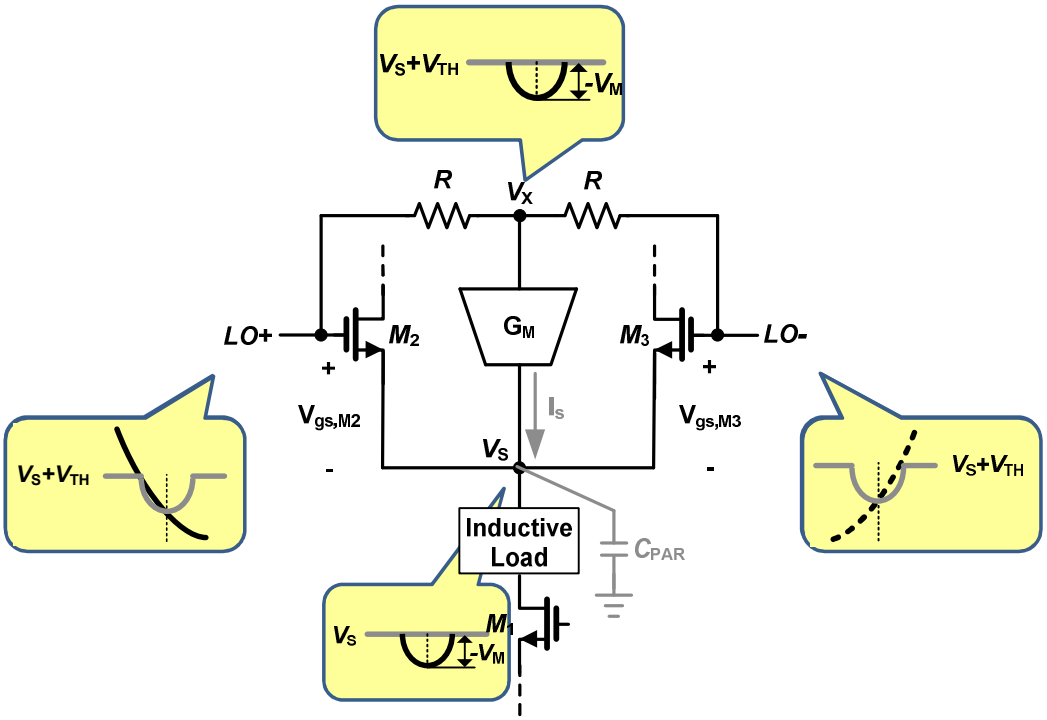


(b)

Figure 5.15 : The compensation process of the proposed mixer. (a) ON overlap mode. (b) OFF overlap mode.

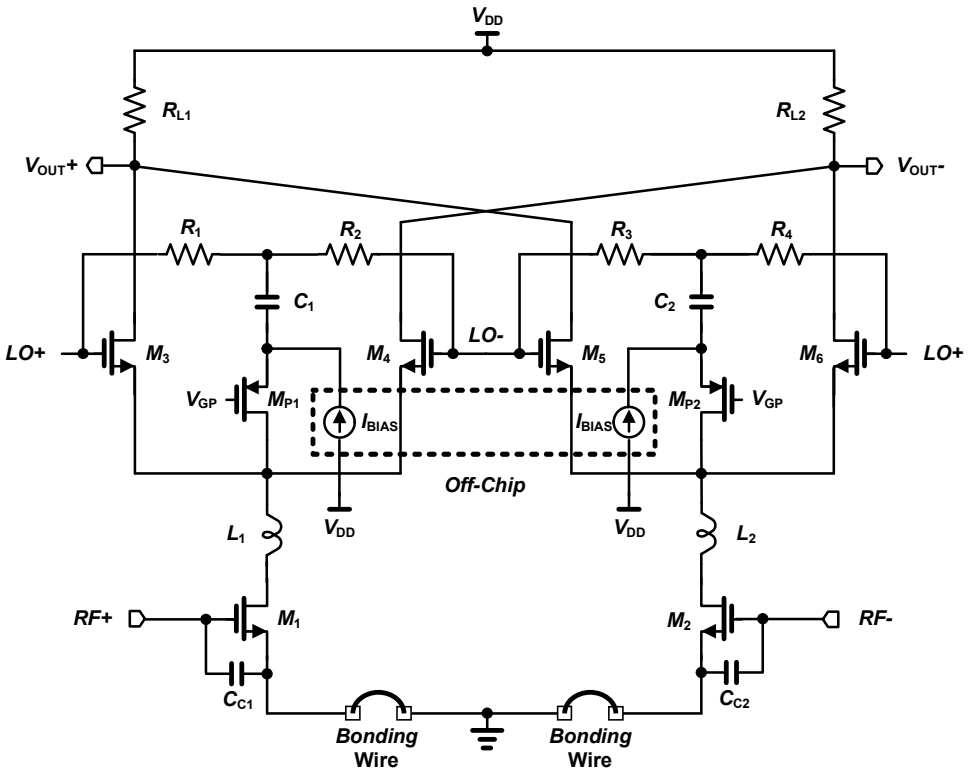


Figure 5.16 : Entire schematic of the proposed idea.

The trans-conductance amplifier is implemented through common gate PMOS transistors, M_{P1} and M_{P2}, whose drains are connected to the common source of the switching pairs in the mixer. To block a DC common mode signal from the output of the detector, DC block capacitors, C_1 and C_2, are used at the source of the PMOS transistors. Thus, to provide DC current paths for PMOS devices, DC bias current sources are implemented by RF chokes, which are employed from the off-chip. The gate DC bias, V_{GP}, and the size of the PMOS devices need to be properly chosen so that the bleeding current of the amplifier is set to be 50% of the total current when the detector doesn't produce AC output voltage. In addition, the size of the PMOS devices should be designed as small as possible to prevent additional parasitic capacitances. The series inductive load

is realized by a small value of inductors, L_1 and L_2. From the simulation results, the 1.2nH of L_1 and L_2, which does not significantly increase total die areas, is enough to separate the parasitic capacitance at the node V_S even when the inductor may not resonate with parasitic capacitance.

5.7. Measurement setup

The proposed mixer is assembled in chip-on-board for utilizing off-chip components. For the differential RF signals of the mixer input, an off-chip balun, 2450BL14C100 from Johnson Technology, is assembled in the board with the mixer. The RF off-chip balun operates from 2.4 to 2.5GHz with single-to-differential conversion. As the RF balun convert from single port impedance of 50Ω to differential port impedance 100Ω, the matching circuits are necessary between the RF balun and mixer input. For the matching circuit and DC blocking, a series connection of an off-chip inductor and a capacitor is inserted.

The precise LO phase mismatch need to be generated for measuring flicker noise of the proposed mixer when it exists. For generating LO phase mismatches, the lengths of LO+ and LO- signal line make different in the PCB board. The required length difference between LO+ and LO- for some values of LO phase mismatch can be easily calculated. The mismatches of LO signal lines and sources except LO signal line in the board needs to be minimized for reliable measurement. To do this, the phase matched balun, 5310A from Picosecond, is used for generating differential LO signal. The phase matched balun has <0.1dB gain mismatch and <0.5 degrees phase mismatches at typical. The lengths of

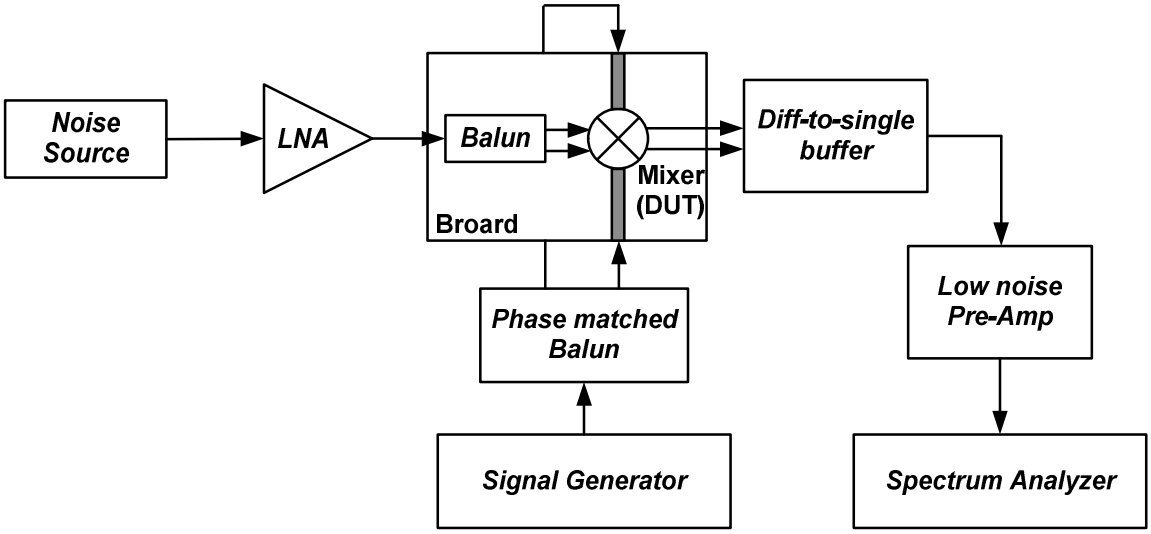


Figure 5.17 : Noise figure measurement setup.

differential lines from the phase matched balun to the board should be same for minimizing additional phase mismatches.

5.7.1 Flicker noise and noise figure measurement setup

The noise measurement of the mixer is performed by Y-factor method, shown in Figure 5.16. To do this, noise source and spectrum analyzer are used at the front-end setup for measuring hot and cold noise factor. A wideband LNA, HMC-C050 from Hittite, is inserted between the noise source and the board. As the wideband LNA facilitates to input matching of the balun, it prevents additional noise generation according to reflected signals. In addition, the gain of LNA is helpful to increase the gap of hot and cold noise factor for precise measurement.

The output of mixer needs to differential to single conversion for measuring at spectrum analyzer. As the conventional balun doesn't operate in very low frequency for direct conversion, a diff-to-single buffer, MAX4444 from Maxim, is used. The diff-to-single buffer provides unit gain and <5KHz flicker noise corner frequency.

The spectrum analyzer, E4440A from Agilent, provides high noise figure, typically >10dB. As the high noise figure of spectrum analyzer prevents precise noise figure measurement, high gain and low noise amplifier with low flicker noise is necessary in front of the analyzer. To do this, the low noise pre-amplifier, 5113 from signal recovery, is utilized. As the pre-amplifier provides high voltage gain in low frequency, the noise from spectrum analyzer can be ignored in noise measurements.

5.7.2 IP3 measurement setup

For making two input tones for IP3 measurements, two signal generators with power combiner are utilized. As the power combiner consists of passive components, the combiner is very linear. These configurations for making two tones do not need to consider any harmonic generation before mixer input.

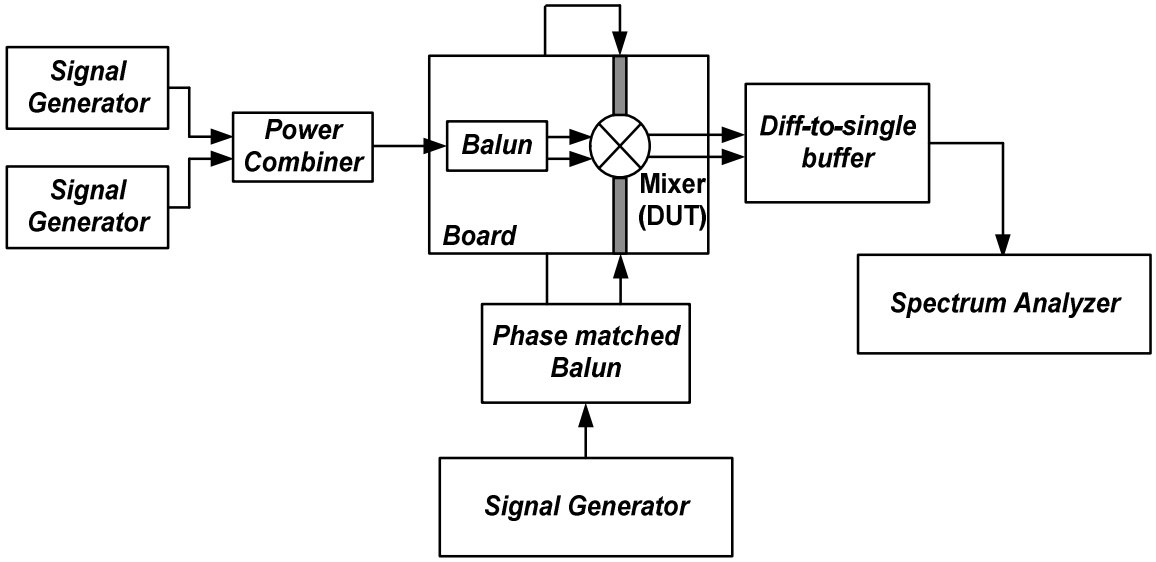


Figure 5.18 : IP3 measurement setup.

5.8. Experimental results

To proof the proposed circuits, a prototype of the proposed mixer was fabricated in 0.18-μm IBM CMOS technology and assembled in chip-on-board. Figure 5.16 shows the die photo for the mixer. The mixer is biased at 7.1mA from a 1.8V supply voltage. The mixer is measured with a sinusoidal LO waveform at frequency of 2.5GHz. The output signal of the mixer is measured at frequency of 1MHz.

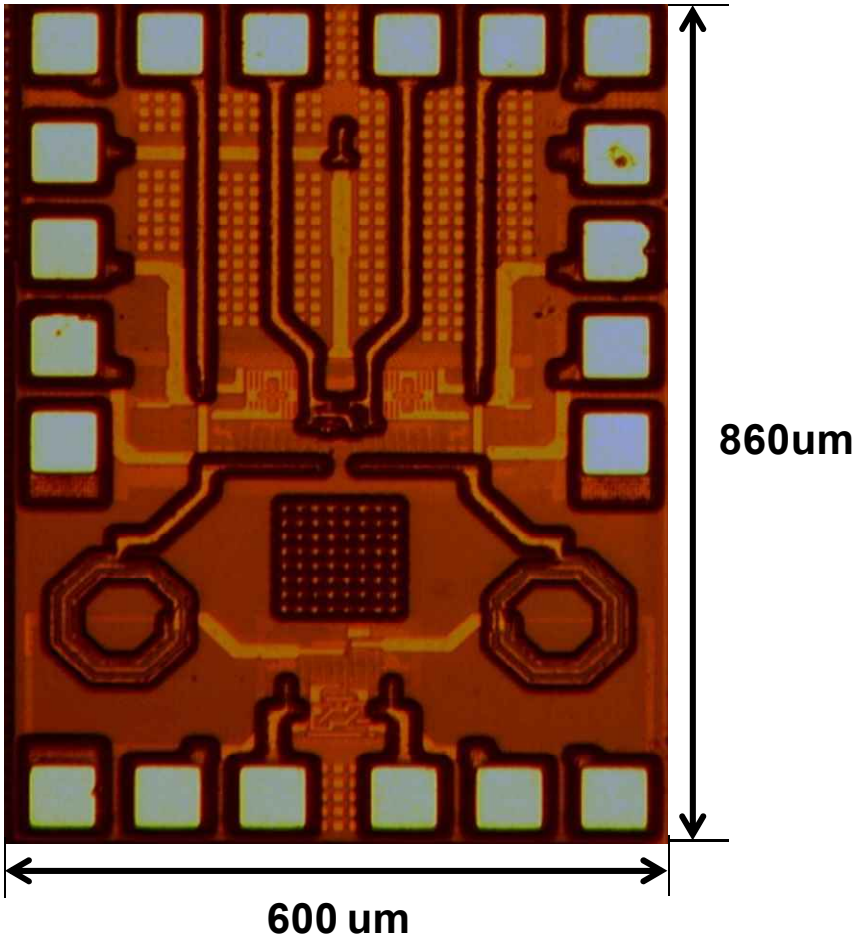


Figure 5.19 : Die photo of the proposed mixer.

Figure 5.20 shows the mixer simulated and measured noise figure over the over the output frequency range of 10 kHz to 10 MHz. A Gilbert-cell mixer with only the current bleeding circuit is also measured for comparative purpose. With the set of 10 degree LO phase mismatch for all mixers, we can observe the phase mismatch compensation performance representing the reduction of flicker noise. For fair comparison of the mixers, the drain to source DC bias voltage of the RF stage and the LO stage are designed to be equal so that all mixers consumes a same current of 7.1mA from a 1.8V supply. In

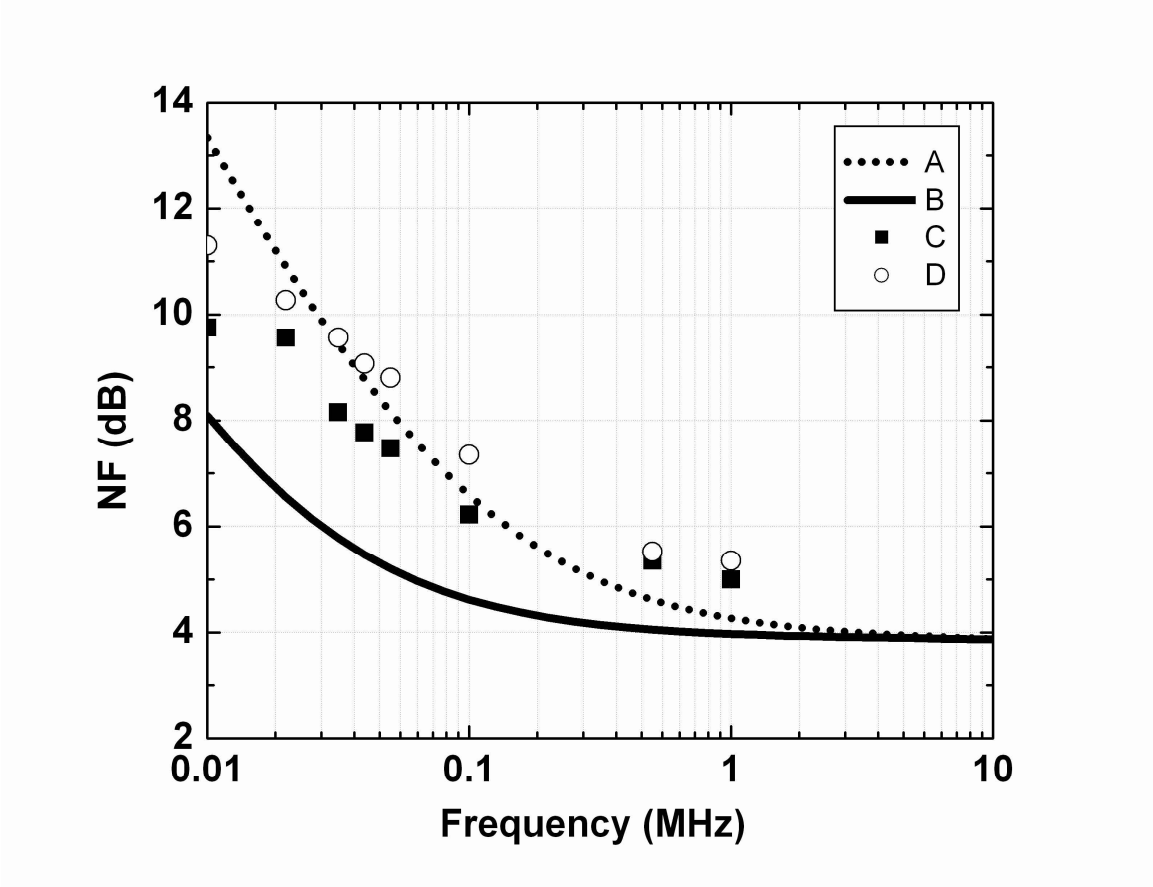
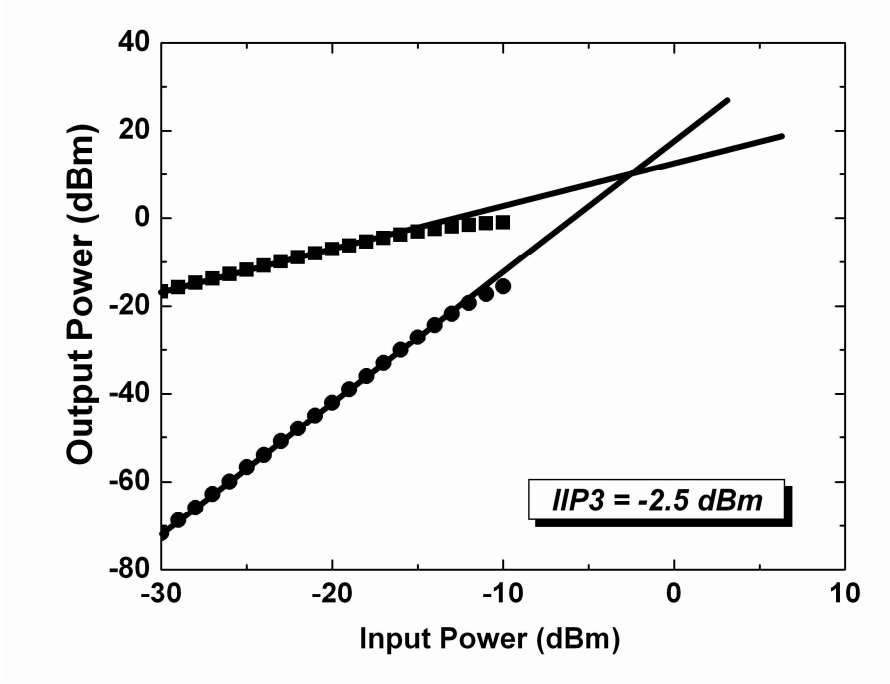
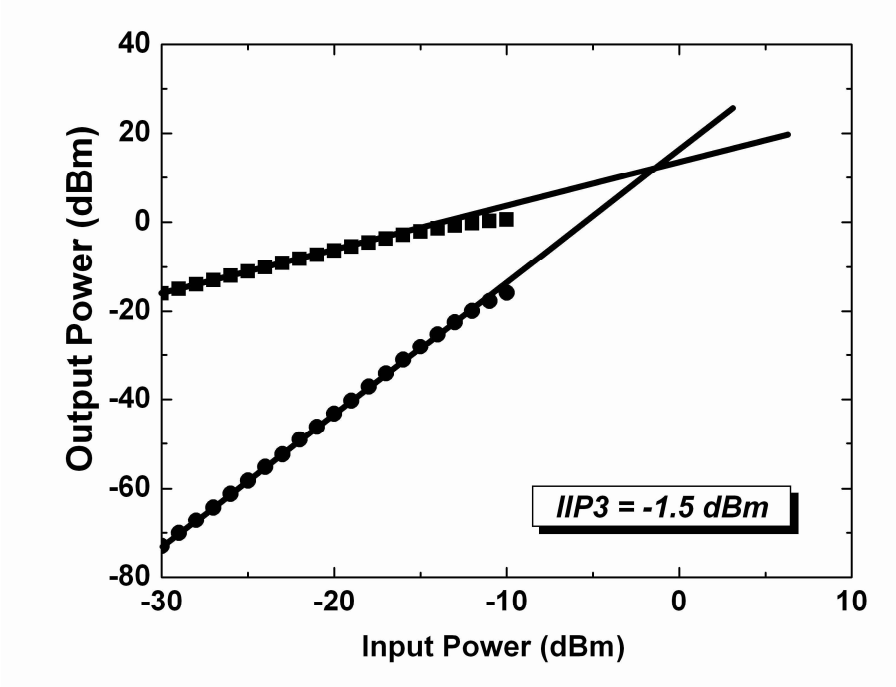


Figure 5.20 : Simulated and measured noise figure at 10' LO phase mismatch. (a) A simulation result of Gilbert-cell mixer with only current bleeding circuit. (b) A simulation result of the proposed mixer. (c) A measured result of the proposed mixer. (d) A measured result of Gilbert-cell mixer with only current bleeding circuit.

simulation results, the proposed mixer has a flicker noise corner of about 40 kHz, whereas the mixer with only current bleeding has that of about 8 MHz. The flicker corner frequency is defined as the frequency converging flicker and white noise. The measured results are also fairly similar with the simulations performance. Both simulation and measured results present that flicker noise due to the LO phase mismatch can be reduced through the proposed topology. In addition, the inductive load plays a great role in partially cancellation of the parasitic capacitance.



(a)



(b)

Figure 5.21 : IIP3 measured results. (a) The Gilbert-cell mixer with only current bleeding circuit. (b) The proposed mixer.

The IIP3 is measured and compared in Figure 5.21. The proposed mixer improves the 1dB of IIP3. Even though IIP3 is mainly limited by the transconductance stage, a small amount of IIP3 can be enhanced by balancing switching pair operations. From the node point between transconductance stage and switching stage, the ON and the OFF overlap time produce different values of parasitic capacitance. The balancing switching pair operation through proposed mixer enhances linearity because it sees the constant value of parasitic capacitance.

The conversion gain, noise figure, and linearity are measured and compared in Table 3 with 10° LO phase mismatch. The proposed mixer has the voltage gain of 14 dB, which yields 0.9 dB greater than original one. The gain enhancement is originated from greatly-reduced the ON and OFF overlap time in the proposed mixer. At the ON overlap time, as the amplified signal from the RF stage goes into V_{OUT}+ and V_{OUT} - ports simultaneously through the mixing process of switching pairs, the differential output may not produce converted signal from the input. In contrast, the signal from the RF stage cannot flow to the output since the switching pairs are turned off at the OFF overlap time. In both cases, as the RF input signal do not convert to the output, the conversion gain is low when phase mismatches exist. The simulated noise figure of the proposed mixer is 4.99 dB, and it is enhanced about 0.36 dB compared to original one. It is because that the thermal noise of switching pairs cannot be seen from the output during no LO phase mismatch.

Table 3 : Summary of the measured mixer performance at 10' LO phase mismatch.

	Current bleeding Gilbert cell mixer	Proposed mixer
Gain	13.09 dB	**14 dB**
NF @ 1MHz	5.35 dB	**4.99 dB**
IIP3	-2.5 dBm	**-1.5 dBm**
Corner frequency	550 KHz	**240 KHz**
Current consumption	7.1 mA	7.1 mA

5.9. Summary

This research verifies that LO phase mismatches contribute to degrade gain, noise figure, and flicker noise performance. From the understanding of these mechanisms, this research proposes a new flicker noise reduction technique in the Gilbert-cell active mixer. The new technique in the mixer senses the LO phase mismatching and compensates its effect with a simple configuration. This techniques leads to improve gain, noise figure, linearity, and flicker noise with the fixed power consumption.

VI. CONCLUSIONS

6.1. Technical Contributions and Achievements

For the purpose of developing low noise CMOS RF receivers for wireless mobile communications, this research provides both the theoretical contributions and the successful implementation of RF receivers. The achievements can be summarized as follows:

1. A wideband differential CG LNA is presented with an arbitrary gm value for input matching. The LNA achieves high voltage gain with a help of gm boosting and large output impedance through the positive-negative feedback technique. It also provides low noise figure by reducing channel noise of the main transistors through the technique. Moreover, all these advantages for the CG LNA can be obtained with low power consumption. The measurement results show 21dB voltage gain, 2dB minimum noise figure, and -3.2dB IIP3 while drawing 2mA from 1.8V supply. The circuit is fabricated in a 0.18 μm CMOS technology.
2. By proposing a new flicker noise model and simulating it within an OFDM PHY layer, this research observe the effect of flicker noise in OFDM systems for the first time. To present this effect, we examine BER performance with flicker noise by generating raw and channel-coded data. The proposed flicker noise model offers more precise results for OFDM systems since the effect of flicker noise on each subcarrier is included.
3. For the first time, this research presents a low flicker noise mixer through the reduction of LO phase mismatching. This research theoretically verifies that the

LO phase mismatch degrades flicker noise performance. In addition, it shows gain, noise figure, and linearity are degraded as well when the LO phase mismatches are exist. The detection and compensation method in the mixer successfully enhances all the performance. The measured results presents 0.9dB of gain, 0.35dB of NF, 1.6dB flicker noise, and 1dB IIP3 improves when it compares the mixer without the proposed technique. All these improvements do not need additional power consumption.

6.2. Future Research Directions

The design of low noise RF receiver integrated circuits has not yet fully matured. Some issues, such as wide bandwidth for LNA and low power consumption for mixer are still remained. In addition, small noise figure in LNA and mixer is essential to fulfill the needs of the next generation wireless communications.

The first challenge in the design of the RF receiver is to minimize power consumption. The designed LNA and mixer are biased from 1.8 V supply voltage in 0.18-μm CMOS technology. The deep submicron design of the circuits is welcome to reduce power consumption. The enhancement of output impedance in the LNA through positive-negative feedback technique may be beneficial to improve its gain and noise figure with low power consumption.

Second, for high-date rate communication systems, the small flicker noise and thermal noise are always indispensible. As the SNR improvement in modem side has limitation, the effort to reduce noise in RF side is important. The circuit design with compound semiconductors, such as GaAs and SiGe, can reduce the noise, but it needs high cost.

Thus, researchers in both academia and industry much devote effort to reduce noise in the CMOS technology.

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[1] **Sanghyun Woo**, Woonyun Kim, Chang-Ho Lee, Kyutae Lim, and Joy Laskar, "A 3.6mW Differential Common Gate CMOS LNA with the Positive-Negative Feedback Technique," *IEEE International Solid-State Circuit Conference (ISSCC) Digest of technical papers*, Feb. 2009.

[2] **Sanghyun Woo**, Jinsung Park, Woonyun Kim, Kyutae Lim, and Joy Laskar, "The Effect of Flicker Noise on OFDM Systems", *Electronics Letters*, submitted

[3] **Sanghyun Woo**, Woonyun Kim, Chang-Ho Lee, Kyutae Lim, and Joy Laskar, "A Low Noise Differential Common Gate CMOS LNA with the Positive-Negative Feedback Technique," *IEEE J. Solid-state Circuits*, in preparation

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[5] **Sanghyun Woo**, Hyungsoek Rue, Jeakon Lee, Changho Lee, Joy Laskar, "Effect of RF Impairments in Transmitter for Future Beyond-3G Communications Systems," *IEEE International Symposium on Circuits and Systems (ISCAS),* May 2006.

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